

## Voltage Rails

Power	Voltage	S0-S2	S3	S4	S5	Ctl Signal
VIN	19V	V	V	V	V	
5VPCU	5V	V	V	V	V	3V5V_EN
3VPCU	3V	V	V	V	V	3V5V_EN
15VPCU	15V	V	V	V	V	3V5V_EN
+3.3VALW	3V	V	V	V	V	STB_ON
+1.2VALW	1.2V	V	V	V	V	STB_ON
5VSUS	5V	V	V			SUSON
3VSUS	3V	V	V			SUSON
1.8VSUS	1.8V	V	V			SUSON
VCC5	5V	V				MAINON
VCC3	3V	V				MAINON
VCC2.5	2.5V	V				MAINON
VCC1.8	1.8V	V				MAINON
VCC1.5	1.5V	V				MAINON
VCC1.2	1.2V	V				MAINON
CPU_VDDA	2.5V	V				MAINON
VCC_NB	1.2V	V				MAINON
SMDDR_VTERM	0.9V	V				MAINON
VCC_CORE	By CPU	V				VR_ON
VCC1.1	1.1V	V				MAINON

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 Page 43: SCREW HOLE & EMI  
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## PCI DEVICES IRQ ROUTING

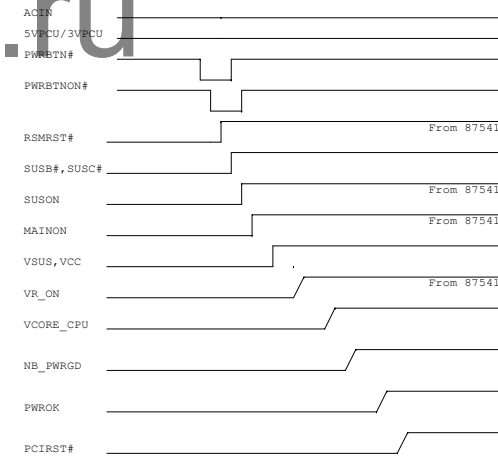
PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts	CLK
NB VGA	NA	A		
SB	AD31(INT)	NA	NA	
AC87/AZALIA	AD31	NA	B	INT
USB	AD30	NA	D	INT
R5C843	AD16	0	E/F/G	PCLK0

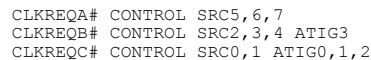
www.aitech1.ru

## PCB STACK UP

LAYER 1 : TOP  
 LAYER 2 : GND  
 LAYER 3 : IN1  
 LAYER 4 : GND  
 LAYER 5 : VCC  
 LAYER 6 : IN2  
 LAYER 7 : GND  
 LAYER 8 : BOT

## Power On Sequence





FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation



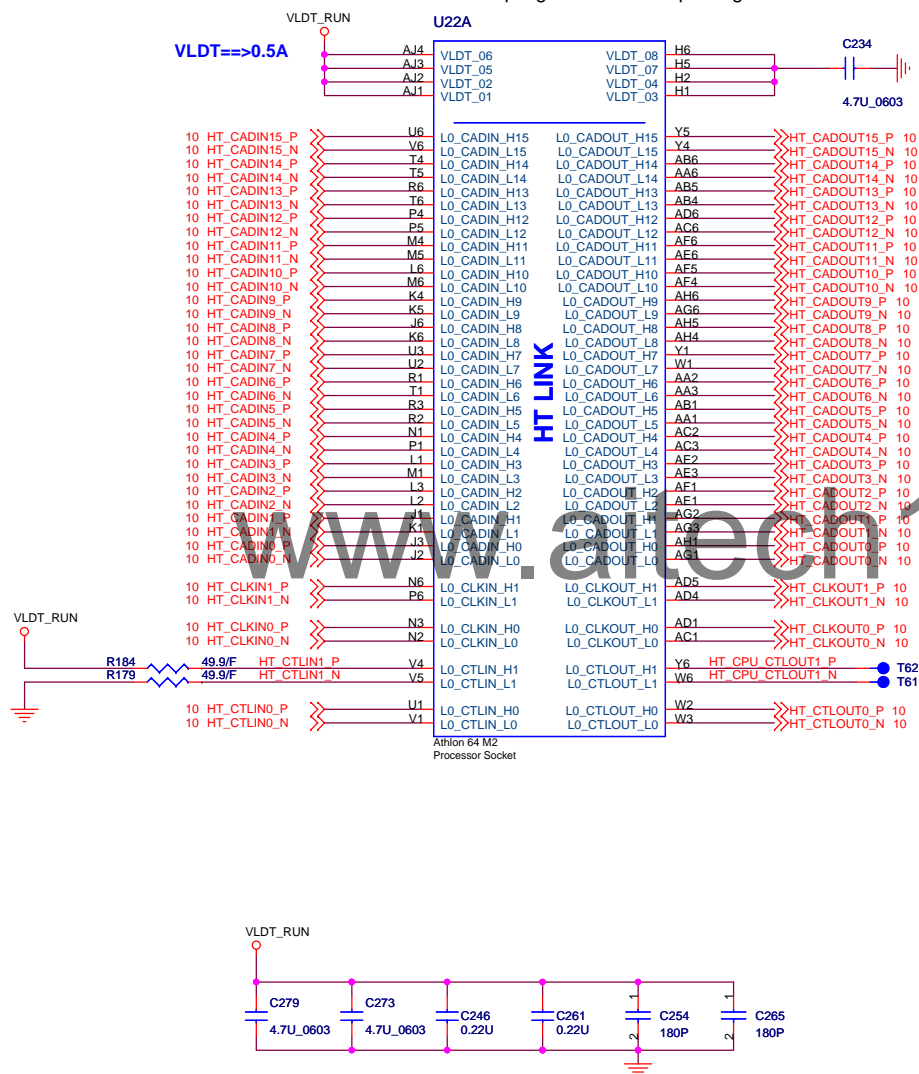
**PROJECT : QU1**

Rev	
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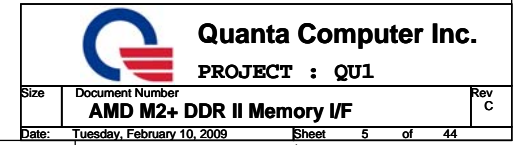
Date: Tuesday, February 10, 2009 Sheet 3 of 44

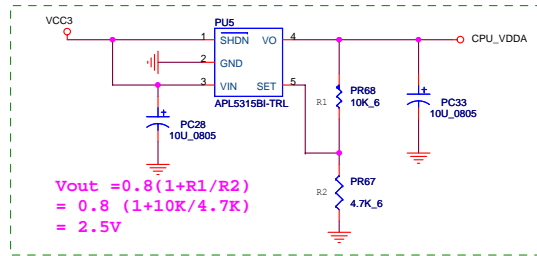
## CPU HyperTransport Interface

VDDLDRUNCPU is connected to the VDD\_LDT\_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



## 5





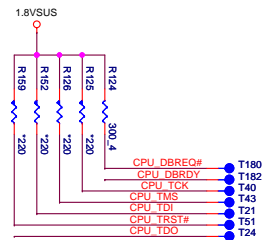
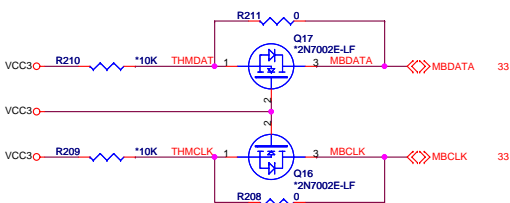
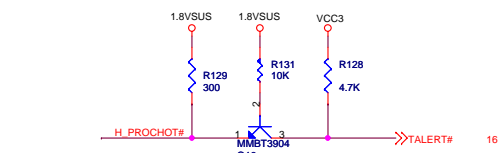
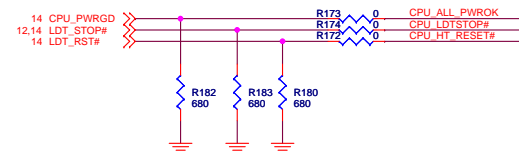
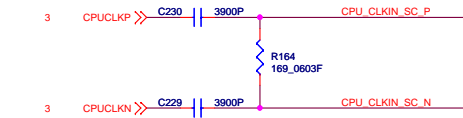
If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- $\Omega$  ( $\pm 5\%$ ) pulldown to VSS.

1.8V SUPPLY

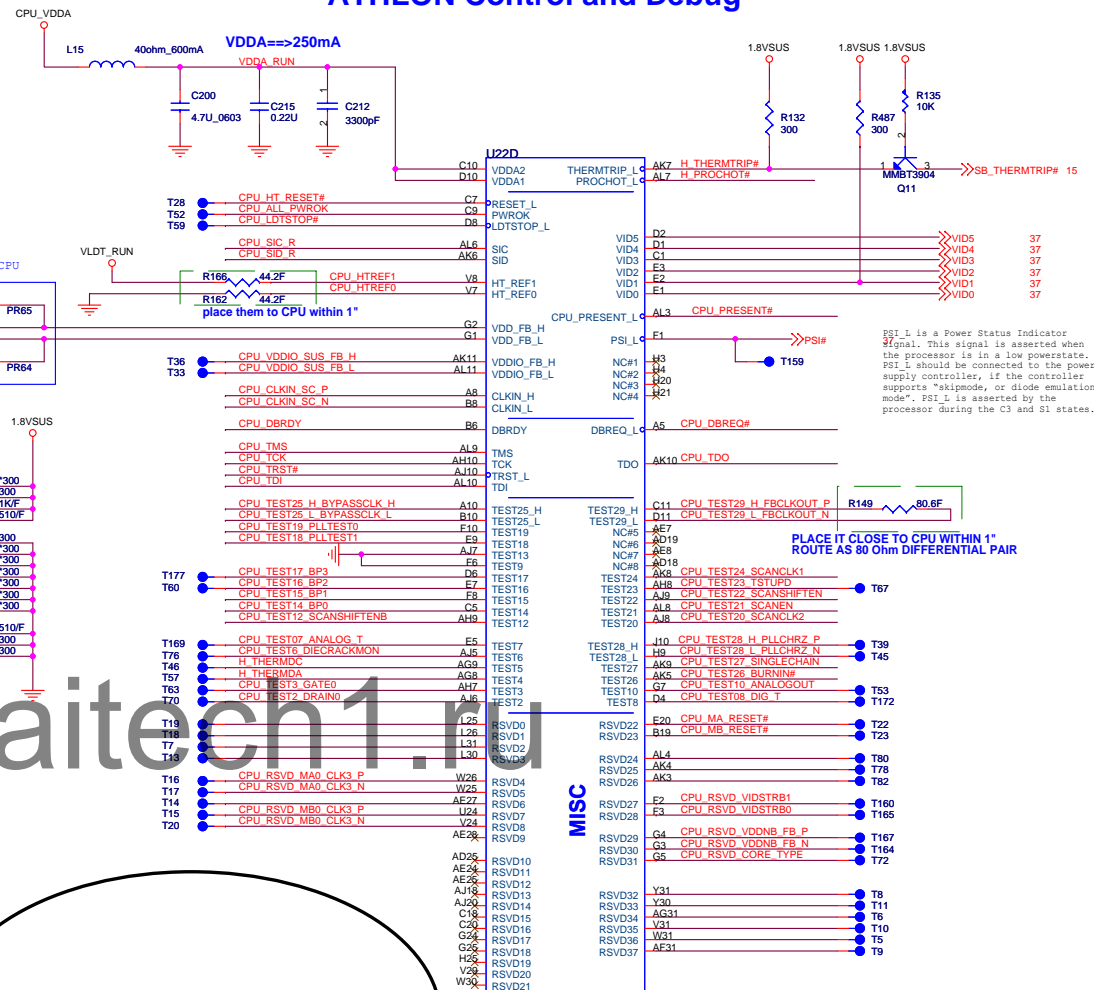
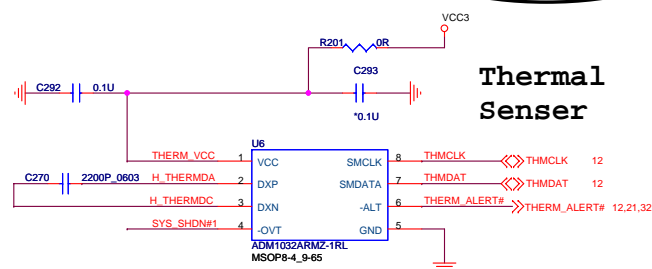
R495 300 R497 300

R501 300

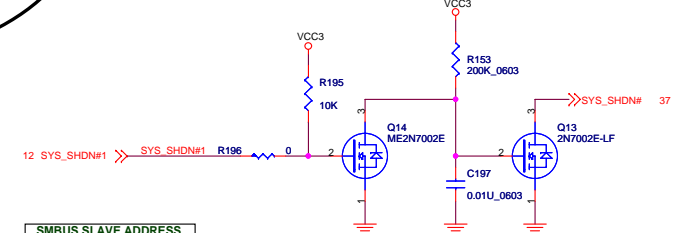
14 CPU\_SIC CPU\_SID CPU\_SIC CPU\_SID



**NOTE: HDT TERMINATION IS REQUIRED FOR REV. Ax SILICON ONLY.**



AMD NPT M2 SOCKET  
Processor Socket

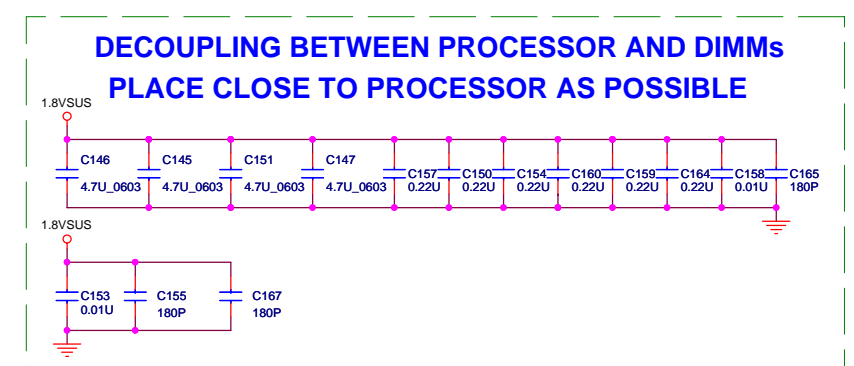
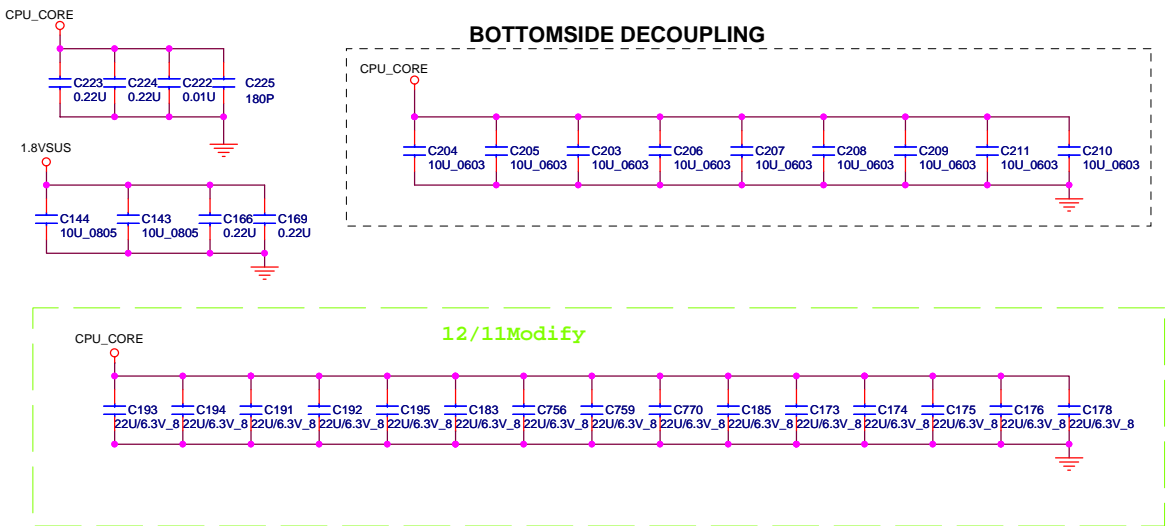
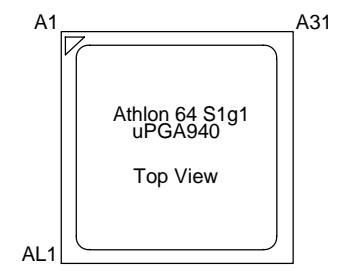
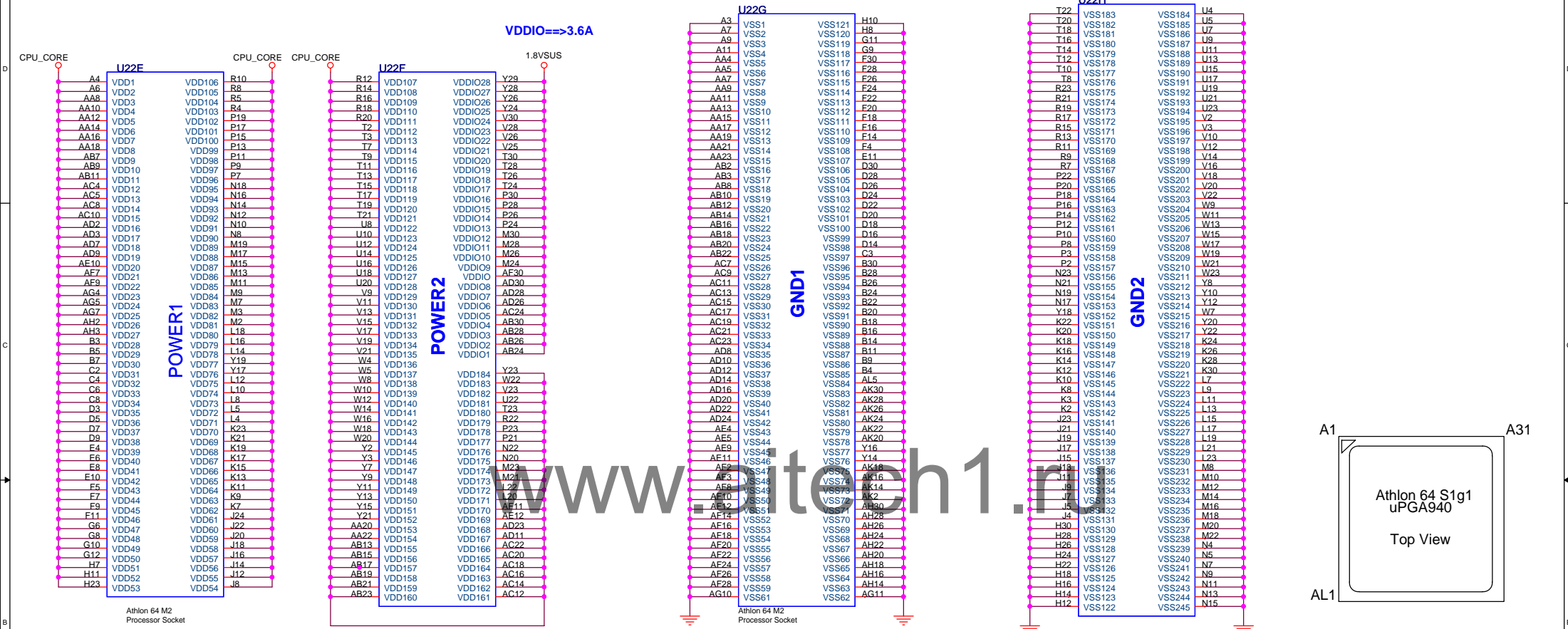


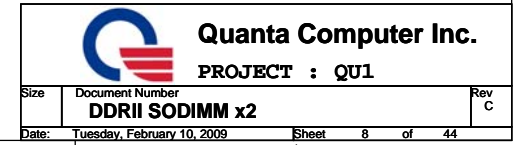
SMBUS SLAVE ADDRESS	
G781	98 (NB)
G781-1	9A (CPU)



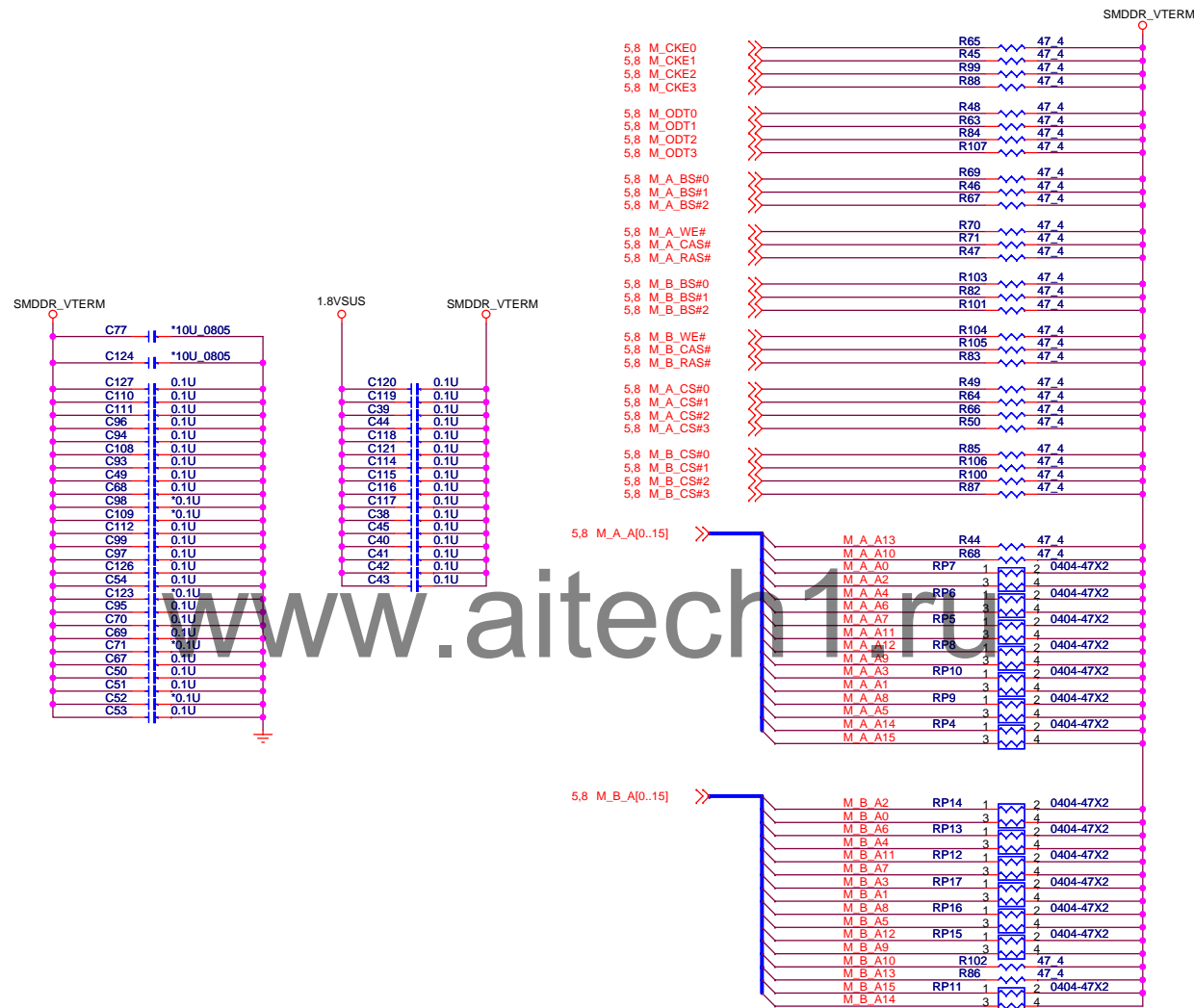
# PROCESSOR POWER AND GROUND

7



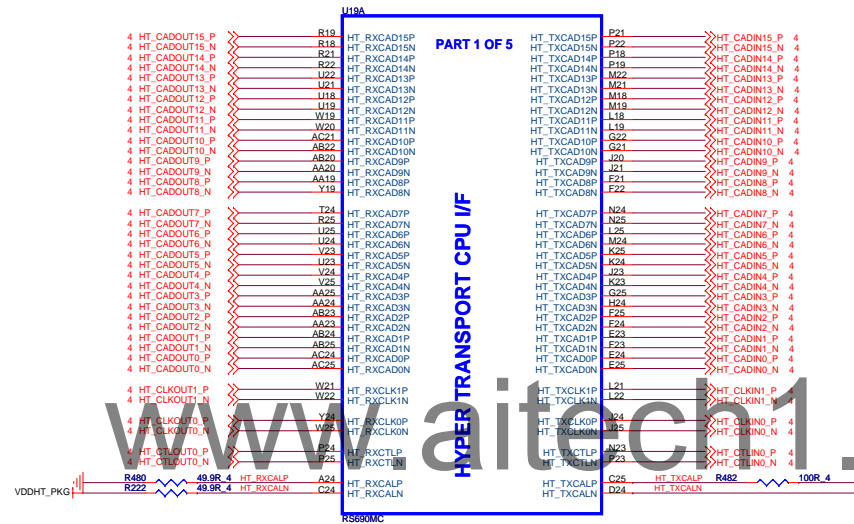


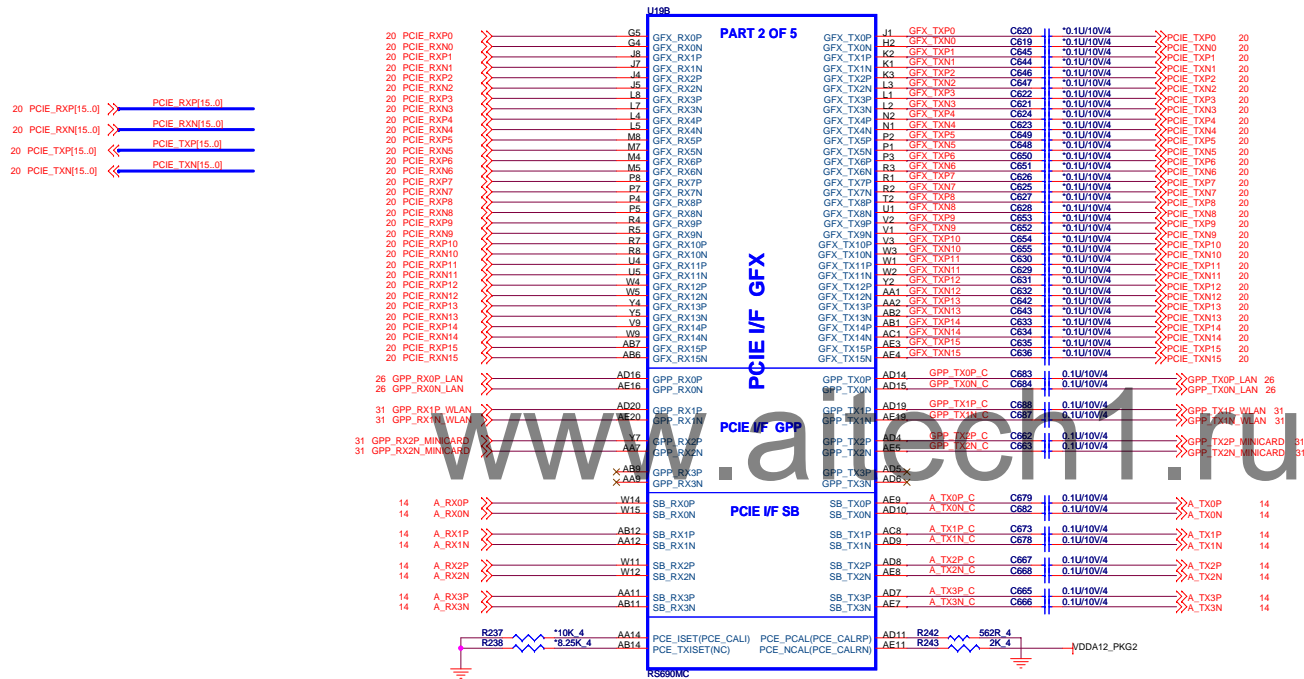


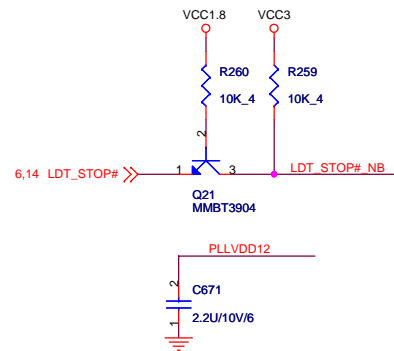
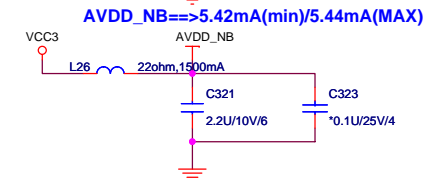
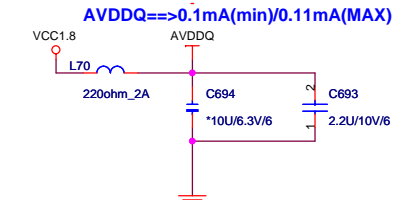
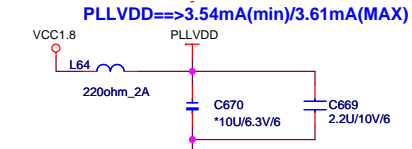
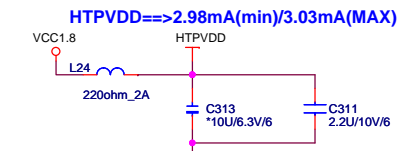


**Quanta Computer Inc.**

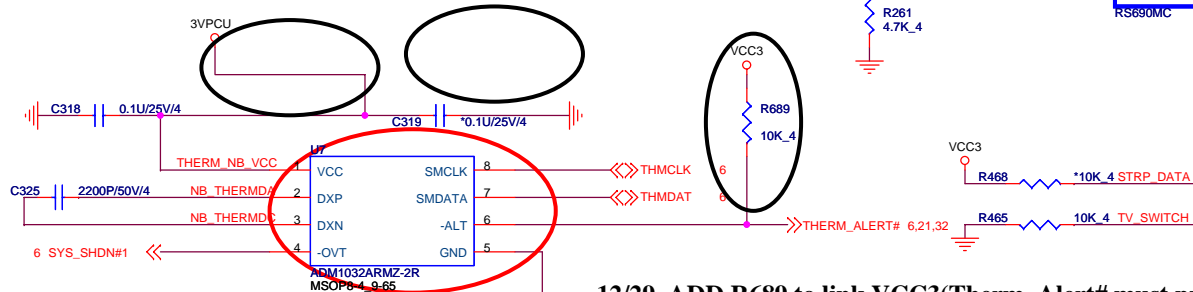
**PROJECT : QU1**





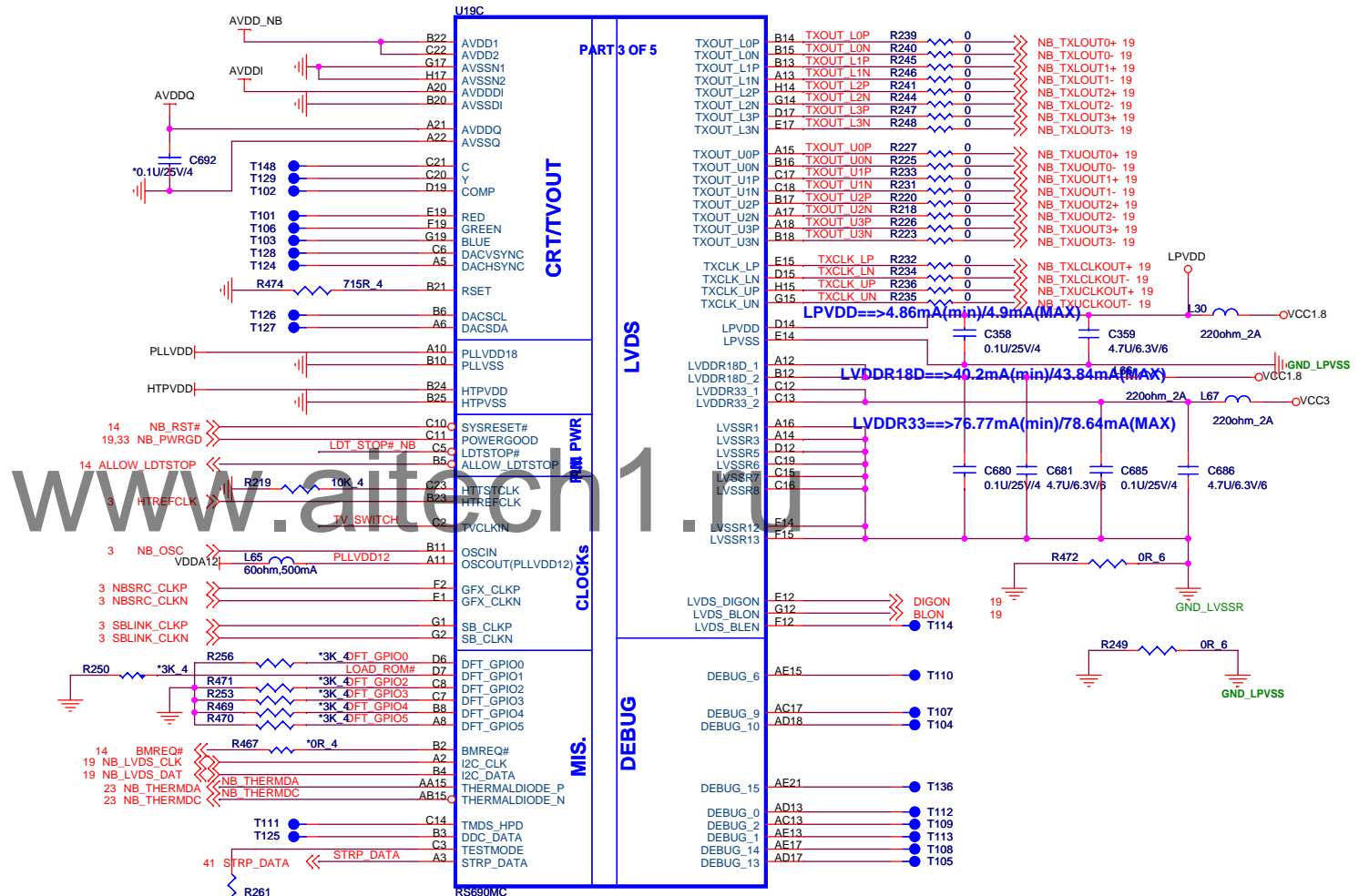


## NB Thermal Sensor



12/02 change U7 P/N:AL001032002

12/29 ADD R689 to link VCC3(Therm\_Alert# must push Hi)



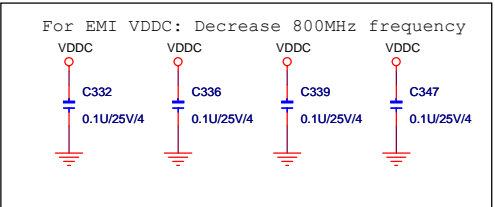
LOAD\_ROM#: LOAD ROM STRAP ENABLE

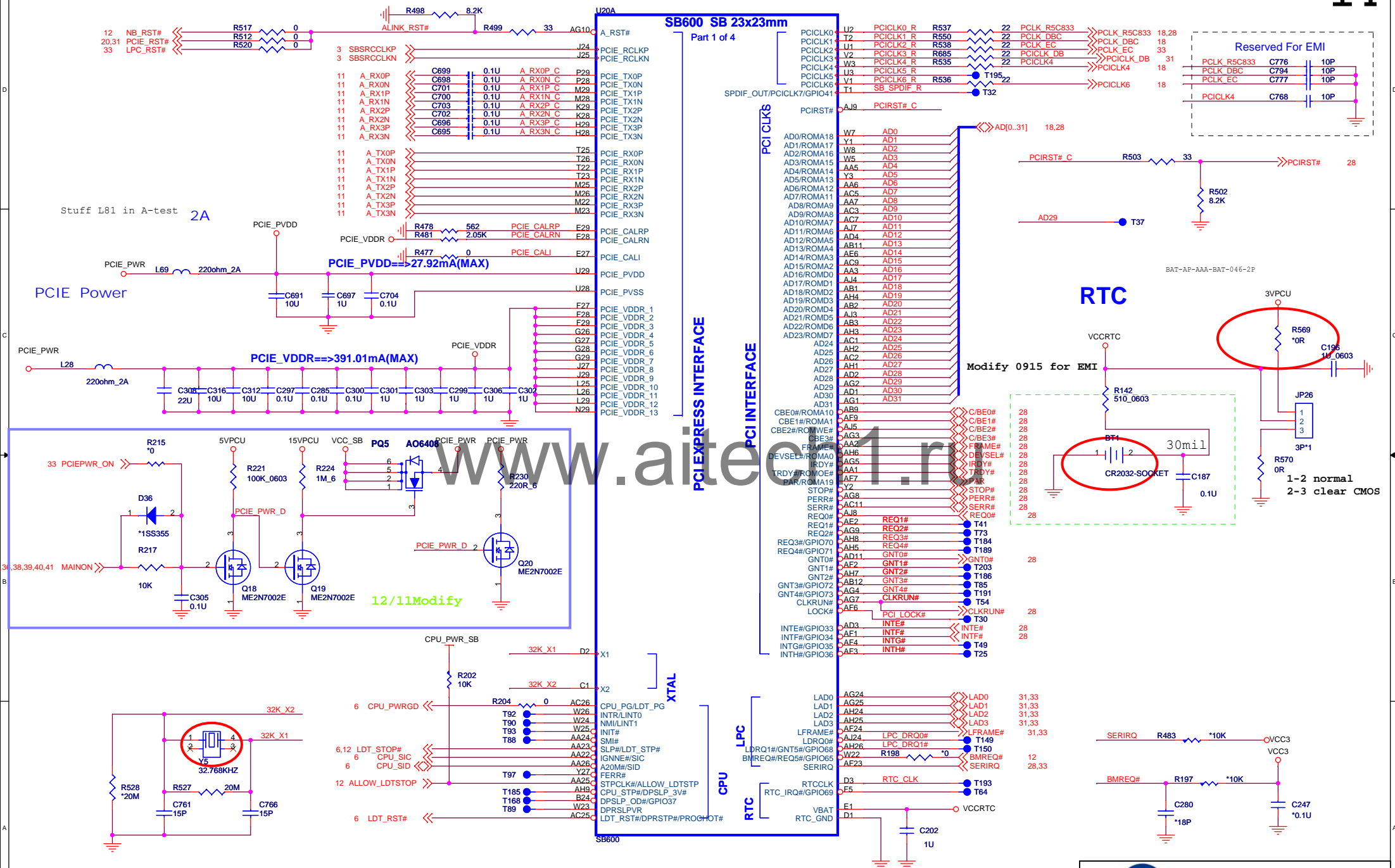
High, LOAD ROM STRAP DISABLE  
Low, LOAD ROM STRAP ENABLE



**Quanta Computer Inc.**

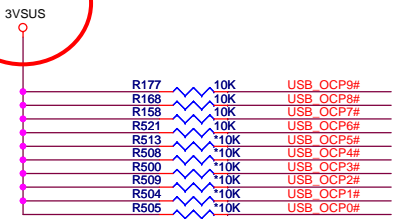
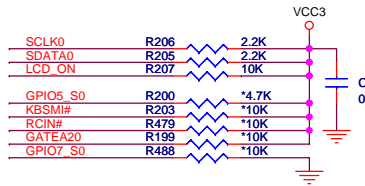
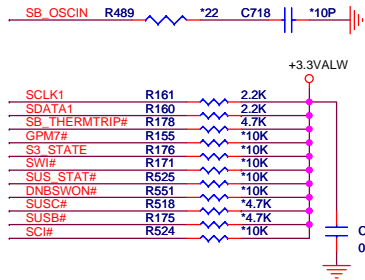
**PROJECT : QU1**



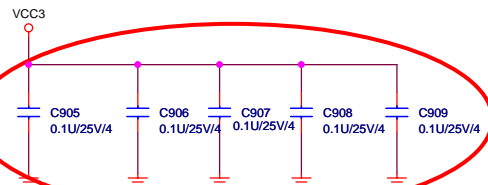
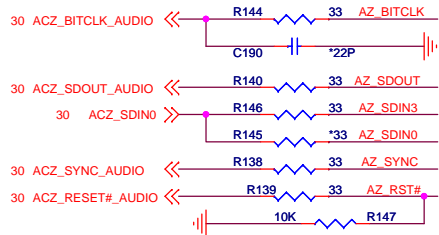


12/01 Change Y5 footprint like Y1 (XTAL-8\_4X3\_7-5\_5X2\_8)

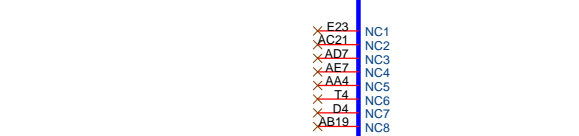
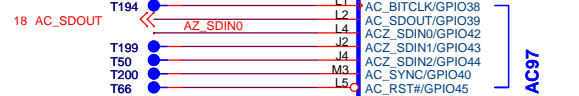
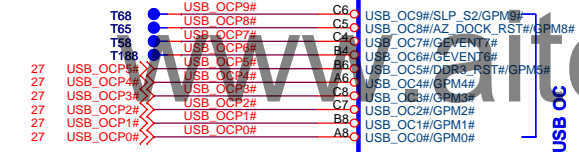
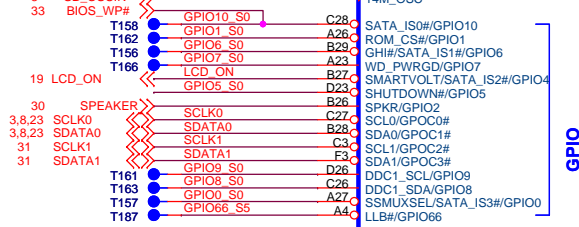
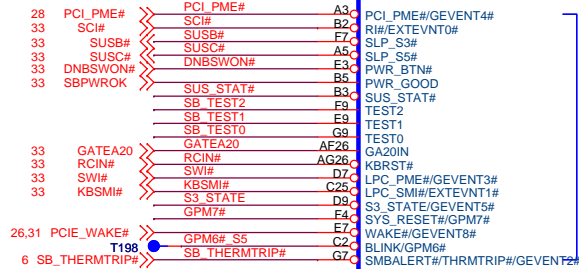




12/05 change USB Power from Vcc3 to 3VSUS



12/10 add xxxxxxxx



SB600 SB 23x23mm

Part 4 of 4

ACPI / WAKE UP  
EVENTS  
USB INTERFACE

OSC / RST

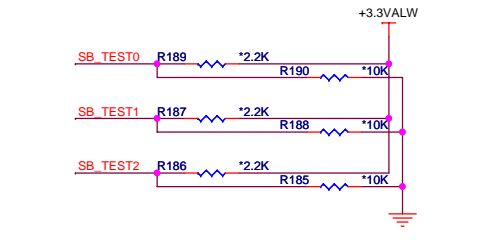
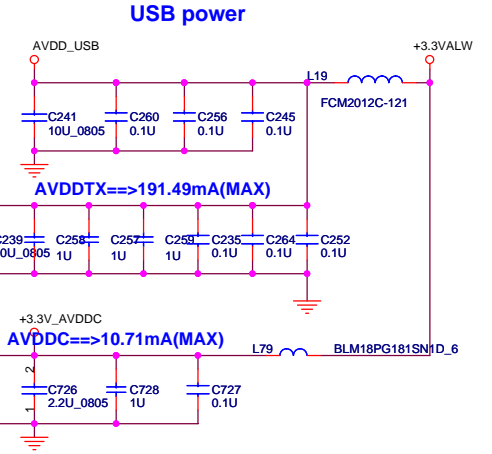
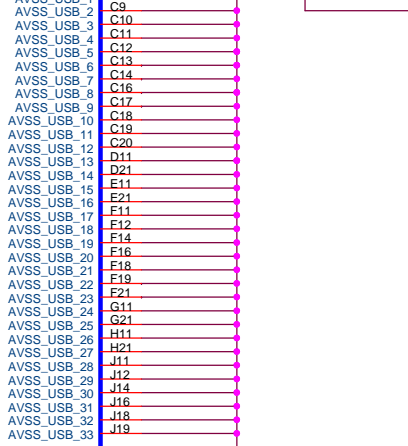
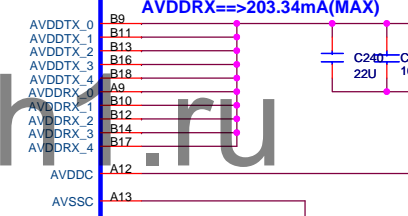
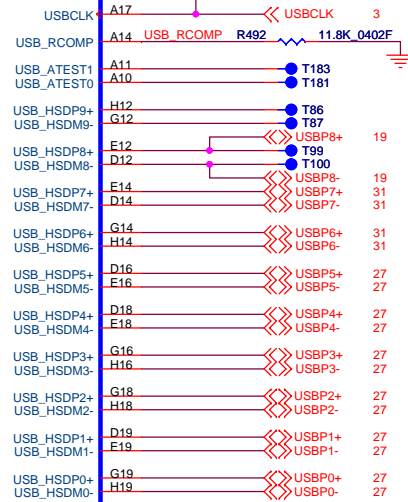
GPIO

USB OC

AZALIA

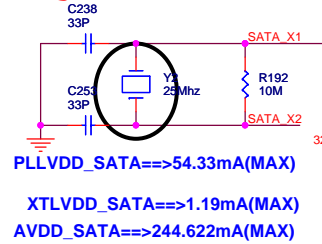
AC97

USB PWR

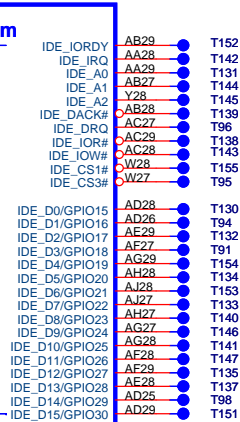
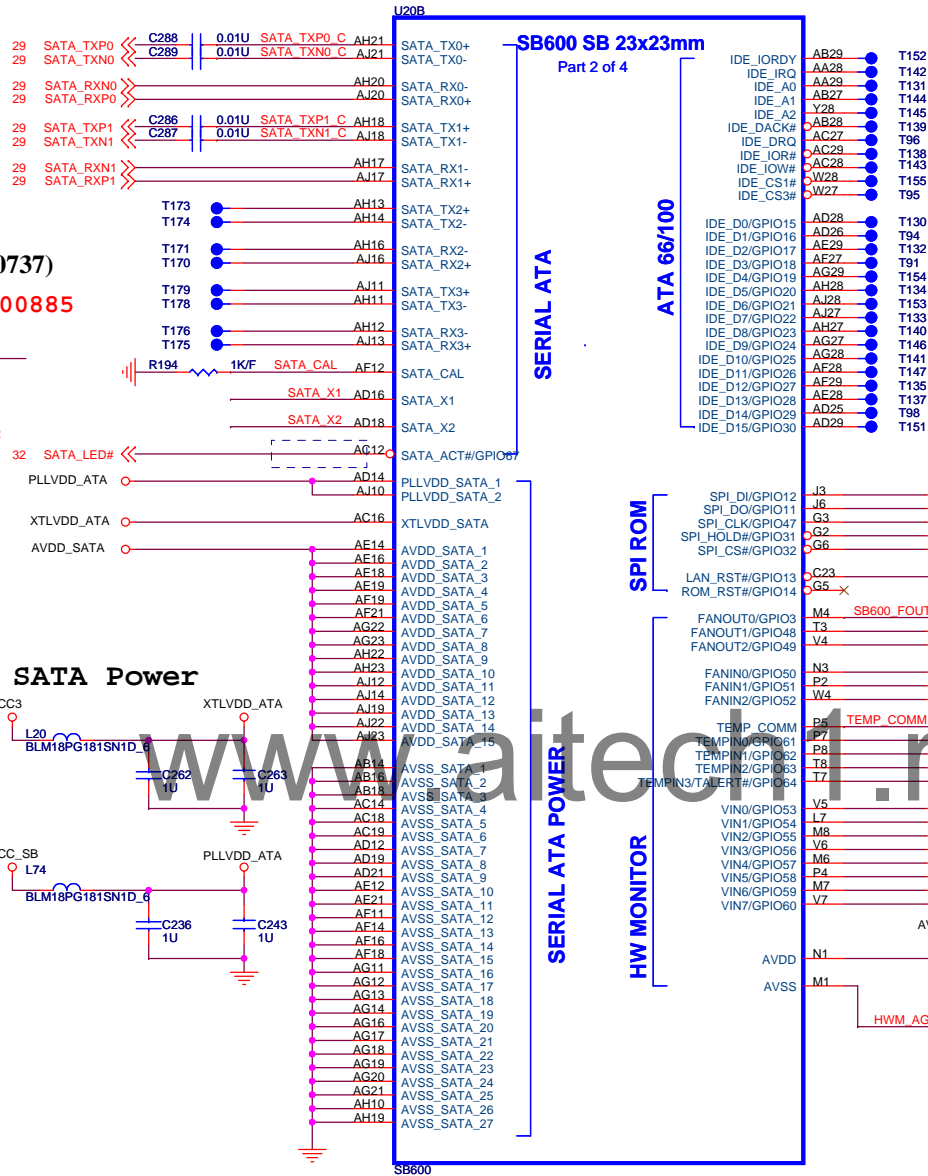
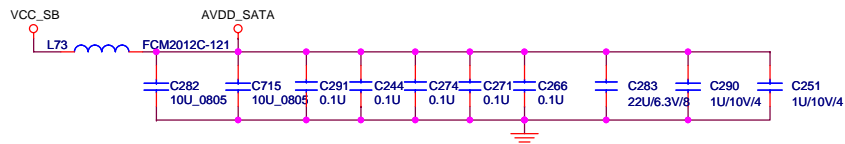
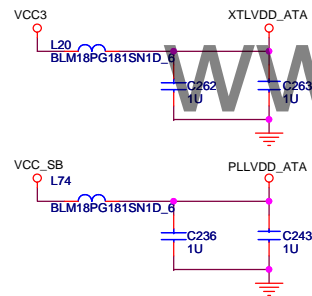


12/26 change Y2 P/N to meet ACL.(BG625000737)

12/02 change Y2 P/N:BG625000885

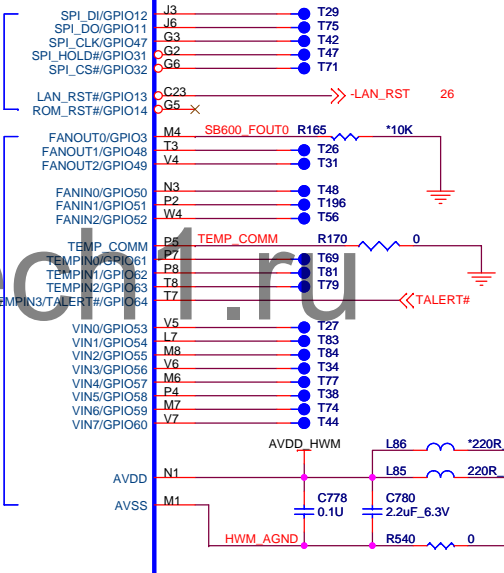


### SATA Power

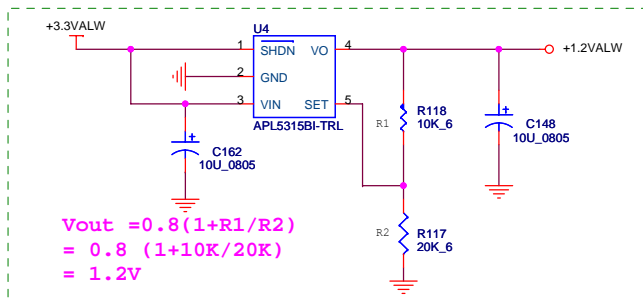
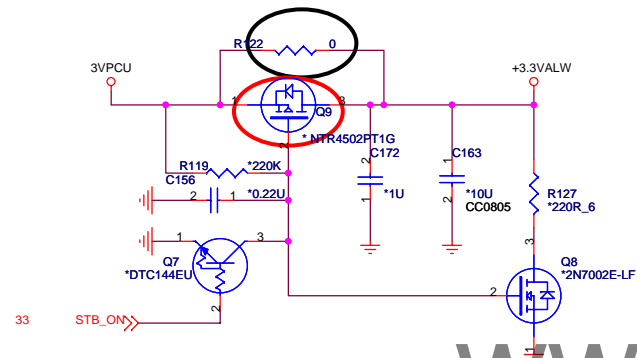


### SPI ROM

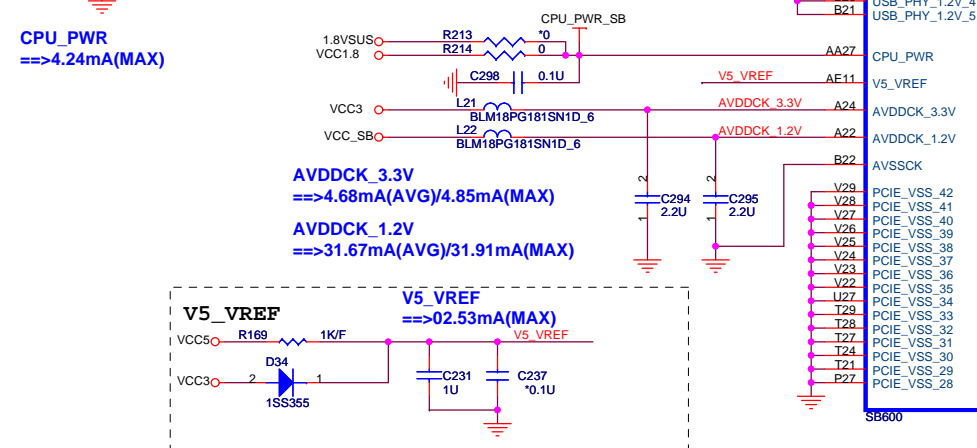
### HW MONITOR



12/21 ADD R122 for HW Lose

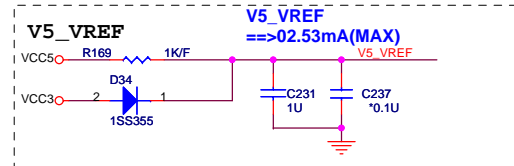


CPU\_PWR  
 $\Rightarrow 4.24mA(MAX)$

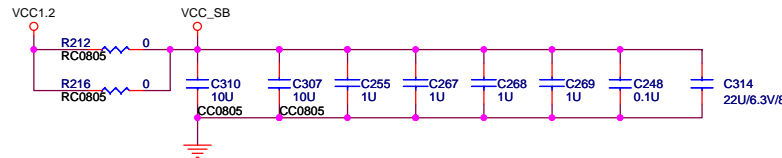


AVDDCK\_3.3V  
 $\Rightarrow 4.68mA(AVG)/4.85mA(MAX)$

AVDDCK\_1.2V  
 $\Rightarrow 31.67mA(AVG)/31.91mA(MAX)$



V5\_VREF  
 $\Rightarrow 02.53mA(MAX)$



VDDQ $\Rightarrow 117.6mA(MAX)$

VDD $\Rightarrow 423.12mA(MAX)$

S5\_3.3V $\Rightarrow 11.03mA(MAX)$

S5\_1.2V  
 $\Rightarrow 70.73mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

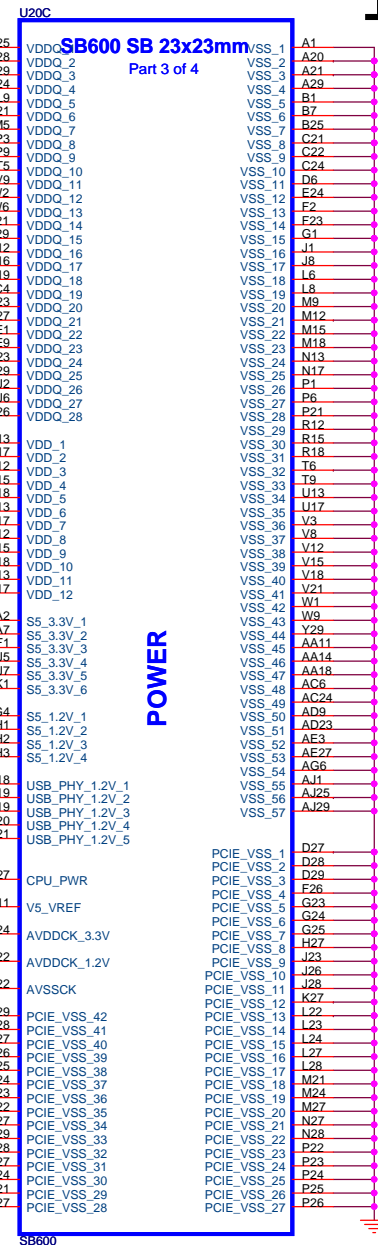
USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$

USB\_PHY\_1.2V  
 $\Rightarrow 77.55mA(MAX)$



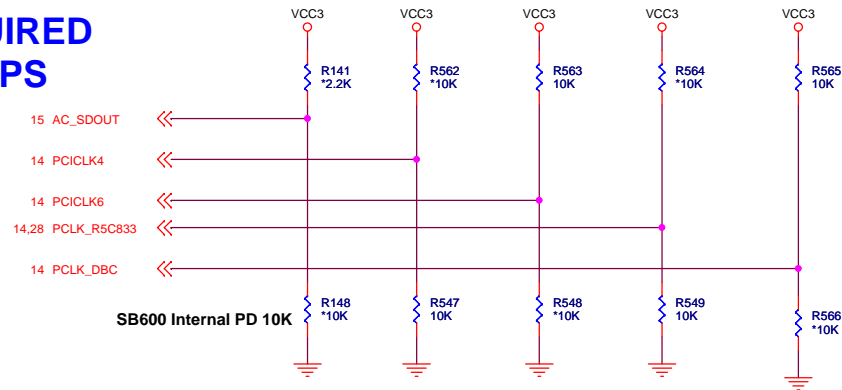
POWER



Quanta Computer Inc.

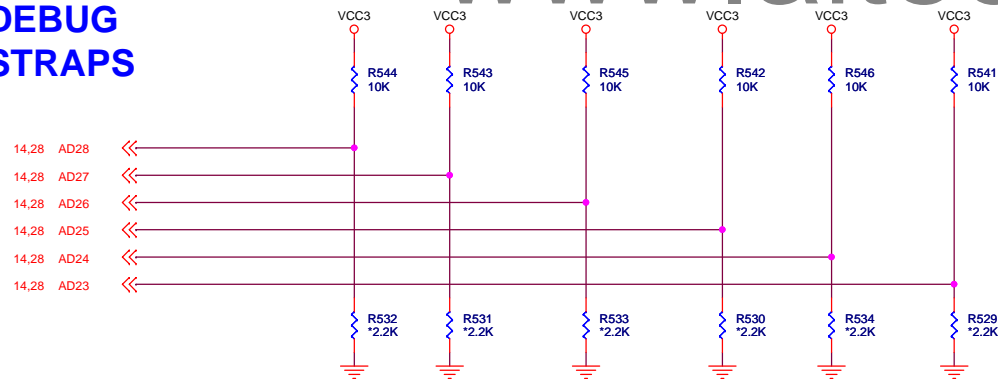
PROJECT :QU1

## REQUIRED STRAPS



	AC_SDOUT	PCICLK4	PCICLK6	PCLK_R5C843	PCLK_DBC
				PCI_CLK0	PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 DEFAULT	ROM TYPE: H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM	DEFAULT
PULL LOW	IGNORE DEBUG STRAPS DEFAULT	USE EXT. 48MHZ DEFAULT	CPU IF=P4		

## DEBUG STRAPS



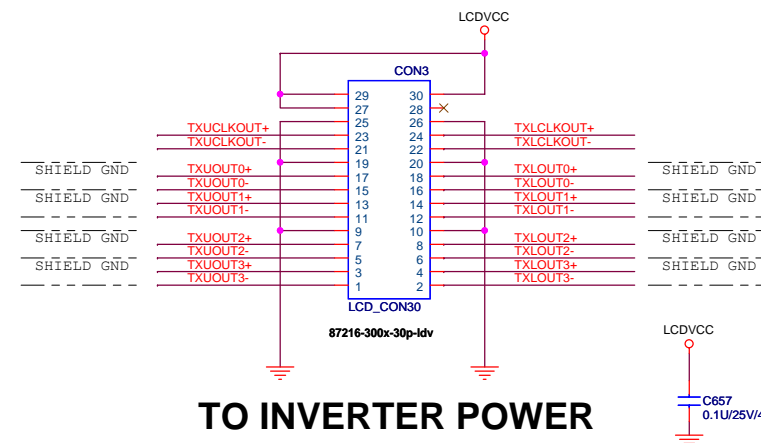
	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	BOOTFAILTIMER DISABLED DEFAULT
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED



**Quanta Computer Inc.**

**PROJECT : QU1**

## 19

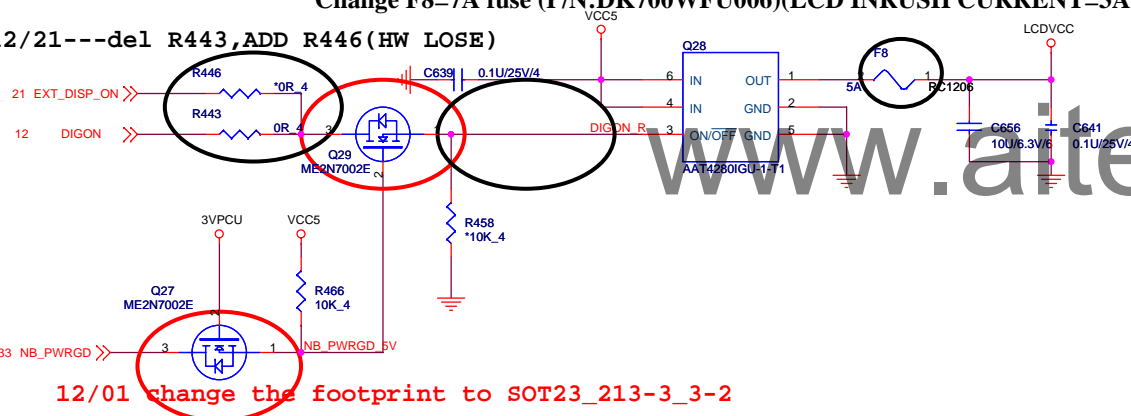


**TO INVERTER POWER**



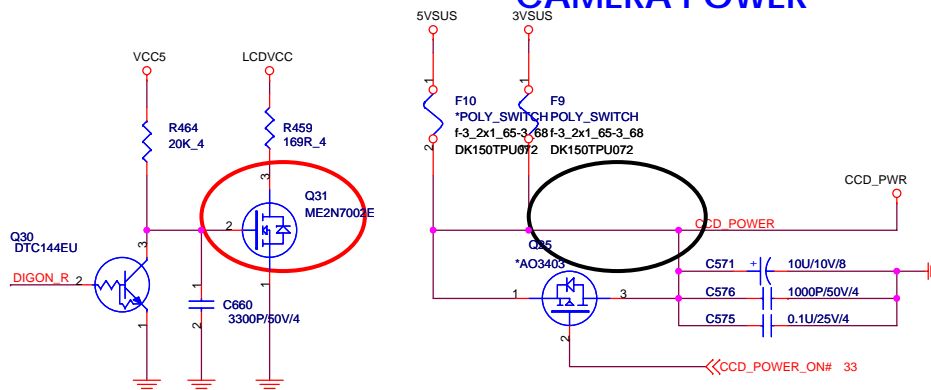
**Change F8=7A fuse (P/N:DK700WFU006)(LCD INRUSH CURRENT=3A)**

12/21---del R443,ADD R446(HW LOSE)

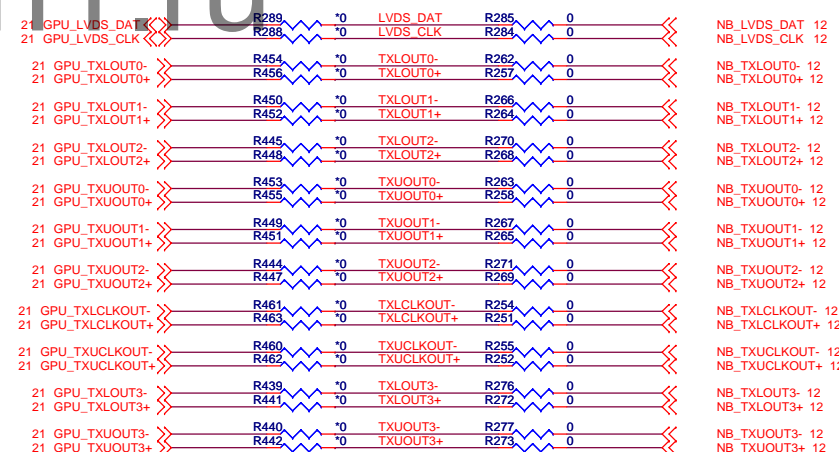


12/01 change the footprint to SOT23\_213-3\_3-2

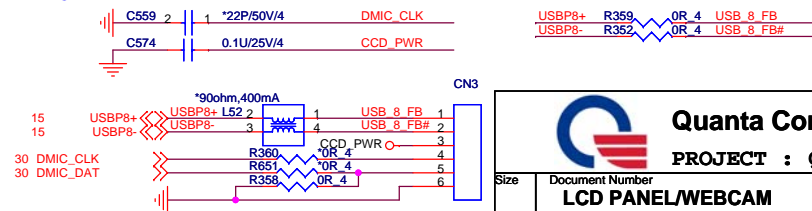
## CAMERA POWER

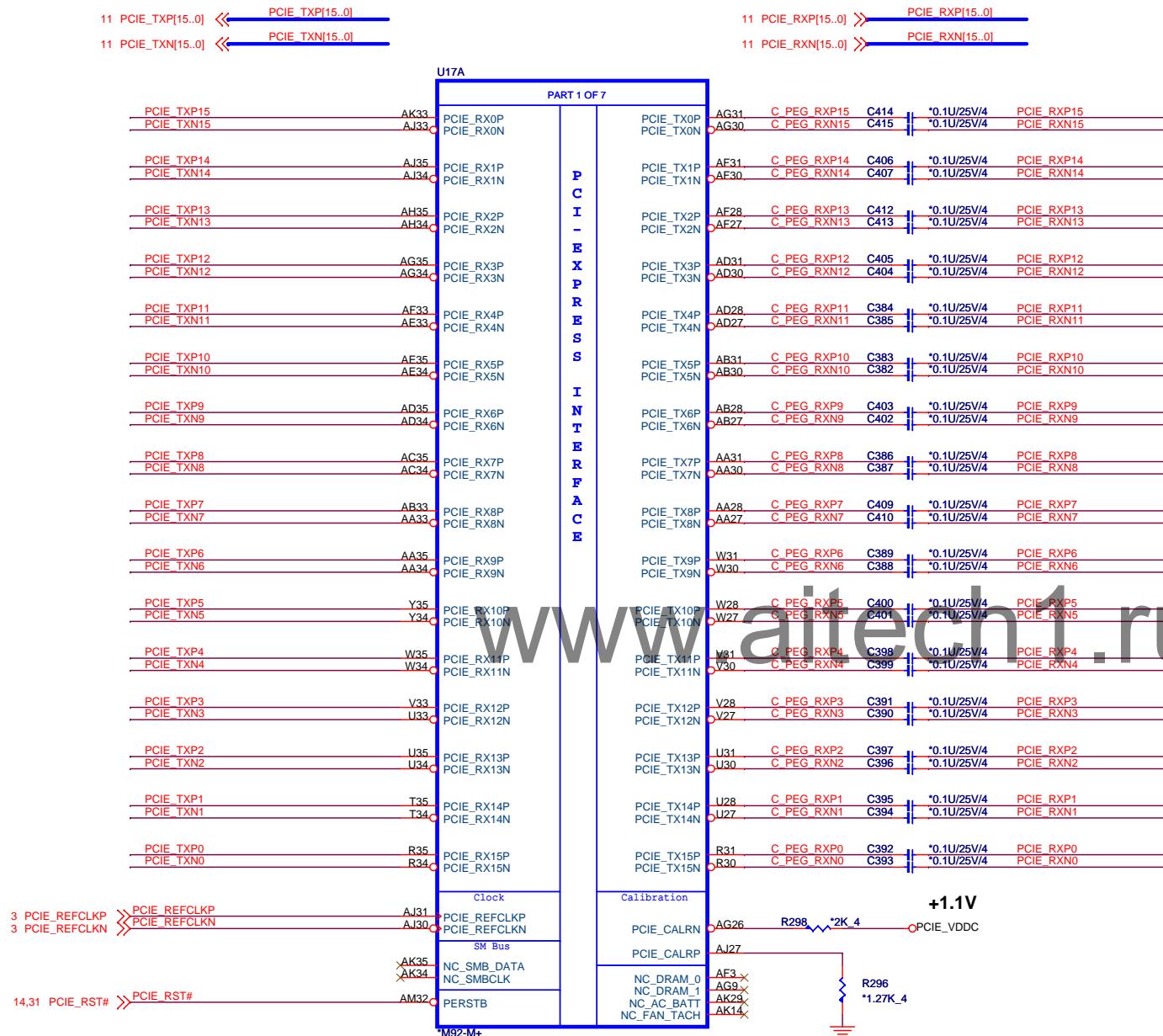


12/01 change the footprint to SOT23\_213-3\_3-2



**FOR EMT WEB CAM MODULE**

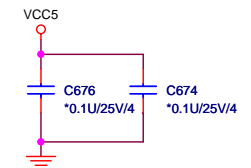




Quantat  
M92-M+ AJ072800T16  
M82-M AJ070700T13

Lenovo  
AJ072800T17  
AJ070700T12

## EMI CAP.

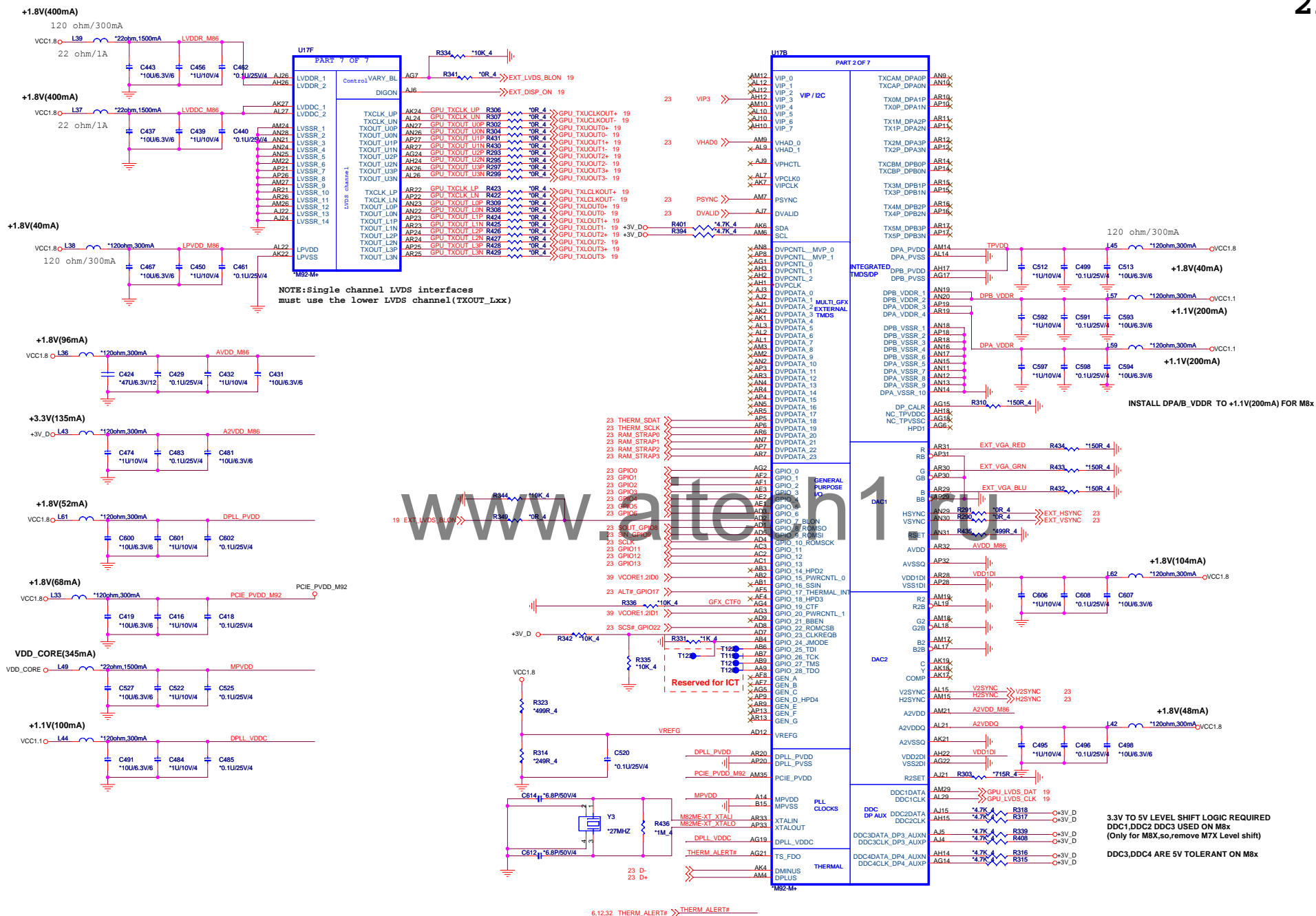


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PROJECT : QUL

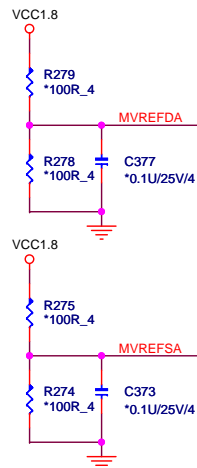
Size	Document Number	Rev
	M82-M PCI-E	A
Date:	Tuesday, February 10, 2009	Sheet 20 of 44





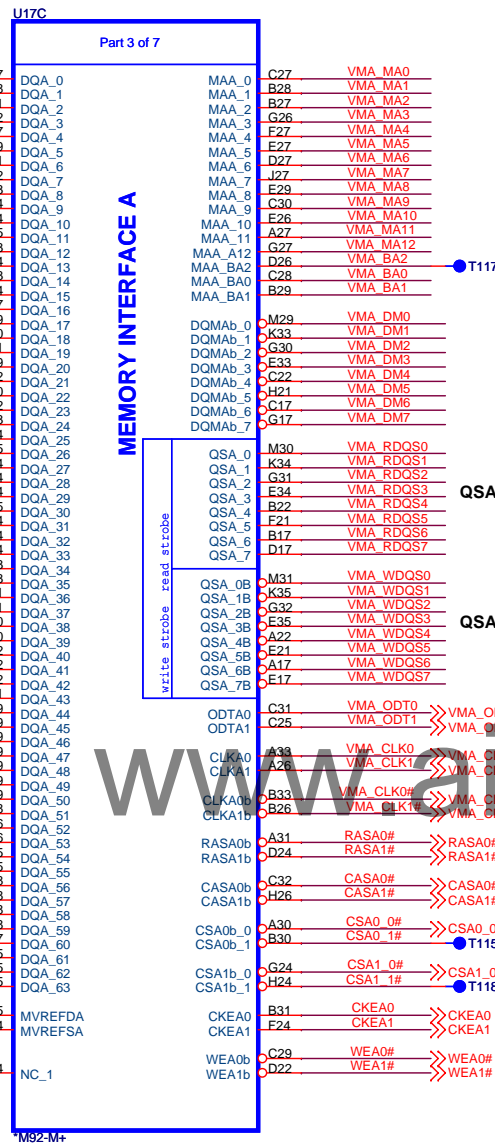
25 VMA\_DQ[63..0] >> VMA\_DQ[63..0]  
 25 VMA\_DM[7..0] >> VMA\_DM[7..0]  
 25 VMA\_RDQS[7..0] >> VMA\_RDQS[7..0]  
 25 VMA\_WDQS[7..0] >> VMA\_WDQS[7..0]  
 25 VMA\_MA[12..0] >> VMA\_MA[12..0]

25 VMA\_BA0 >> VMA\_BA0  
 25 VMA\_BA1 >> VMA\_BA1  
 25 VMA\_BA2 >> VMA\_BA2



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R
MVREF Voltage	0.9V	1.28V

0.5\*VDDQ 0.713\*VDDQ

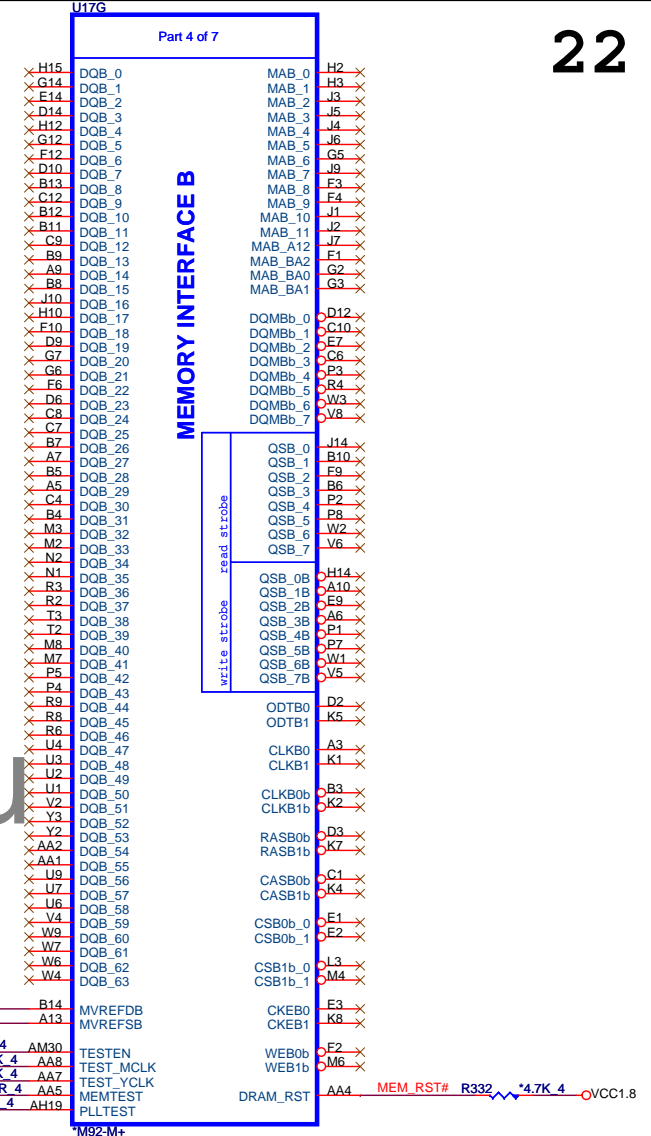
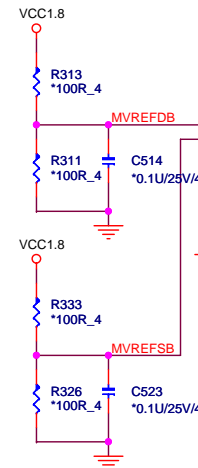


MEMORY INTERFACE A

write strobe read strobe

QSA[7..0]

QSA#[7..0]



MEMORY INTERFACE B

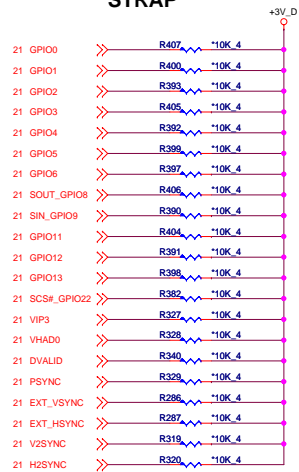
write strobe read strobe

MEM\_RST# R332 \*4.7K 4 VCC1.8

**Quanta Computer Inc.**  
 PROJECT : QU1

Size Document Number  
**M82-M MEMORY I/F**  
 Date: Tuesday, February 10, 2009 Sheet 22 of 44

## STRAP



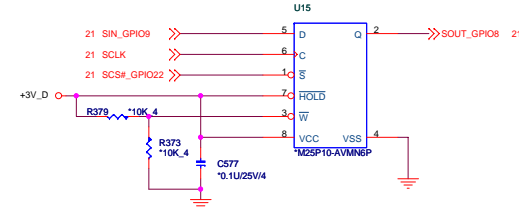
## CONFIGURATION STRAPS

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE RSVD = ATI RESERVED (DO NOT INSTALL)	
			M8s	M7s
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7x/M8x-M)	NA	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MIXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82-S)	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYNC	VGA ENABLED	0	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE, MAKE AND SIZE INFO	X X X X	X X X X

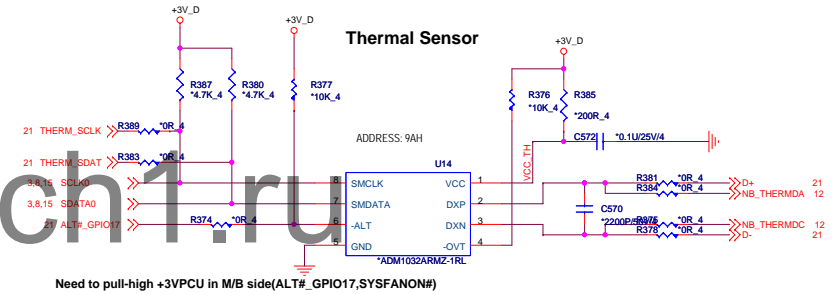
## HDCP FUNCTION

W#	HDCP
0	Enable
1	Disable

## EEPROM



## Thermal Sensor



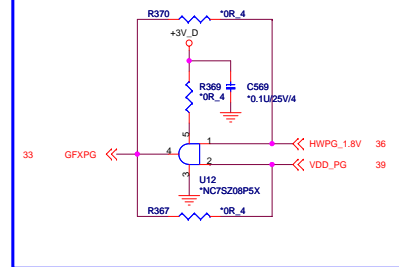
## M86 DDR2 Memory Aperture size

Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (400MHz)	256M	1	1	1	1
Samsung (400MHz)	256M	1	1	1	0

## M82 DDR2 Memory Aperture size

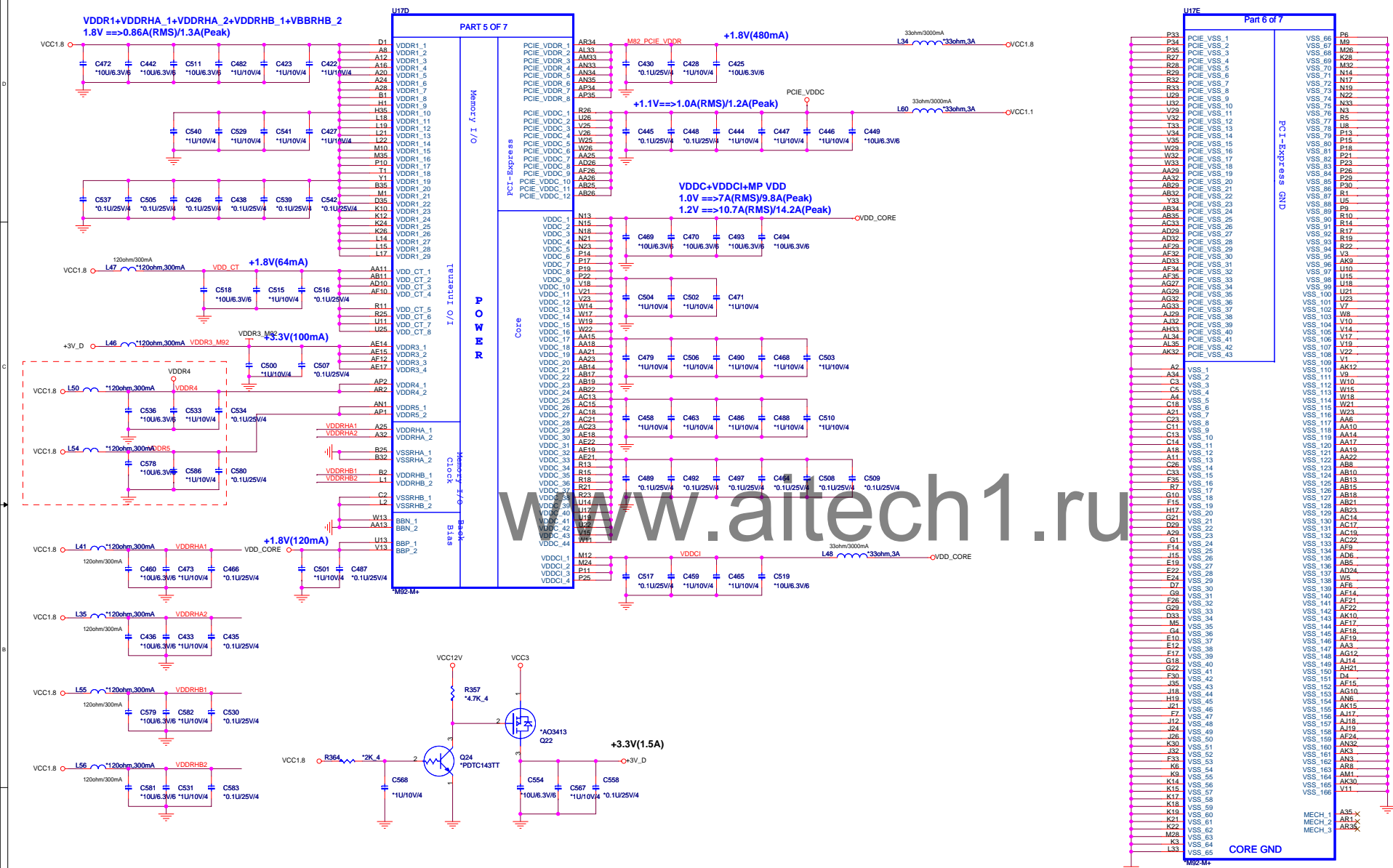
Vendor	Size	RAM_STRAP3 DVPDATA_23	RAM_STRAP2 DVPDATA_22	RAM_STRAP1 DVPDATA_21	RAM_STRAP0 DVPDATA_20
Hynix (500MHz)	512M	1	1	0	1
Samsung (500MHz)	512M	1	0	1	1

## Fine-tune Power-on sequence

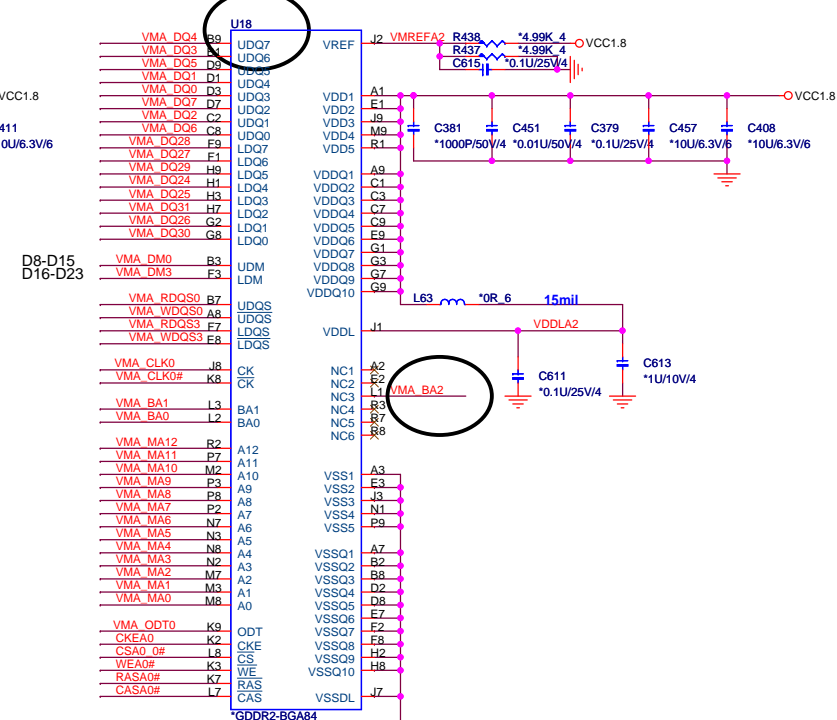
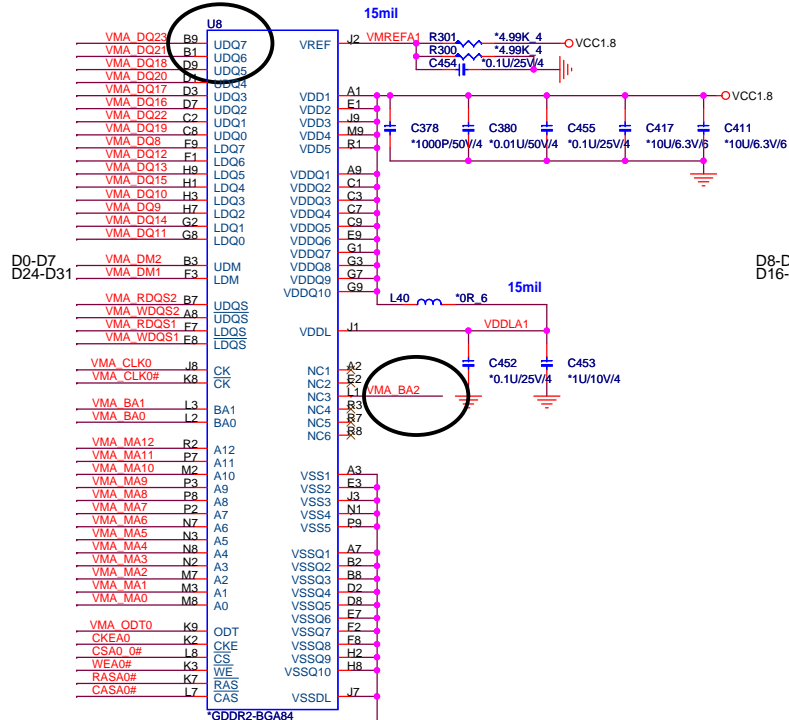
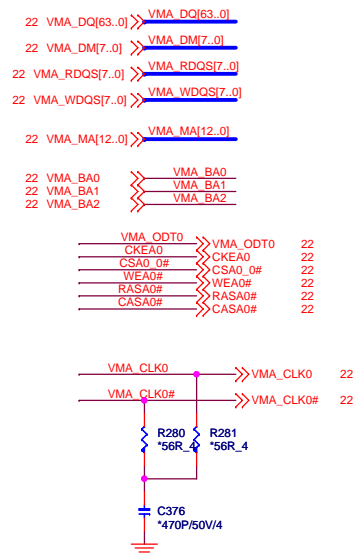


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PROJECT : QU1

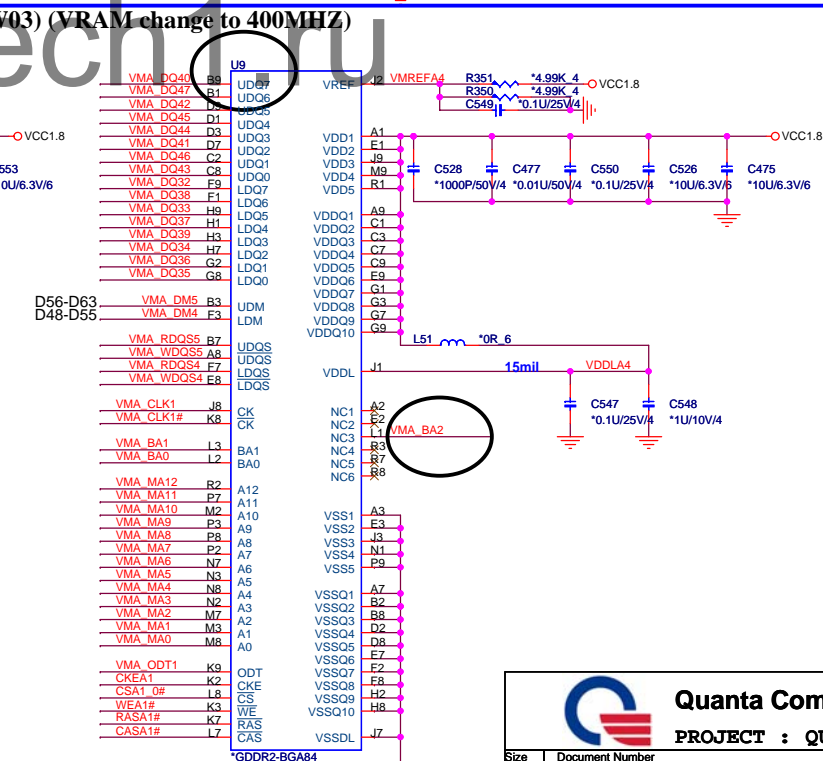
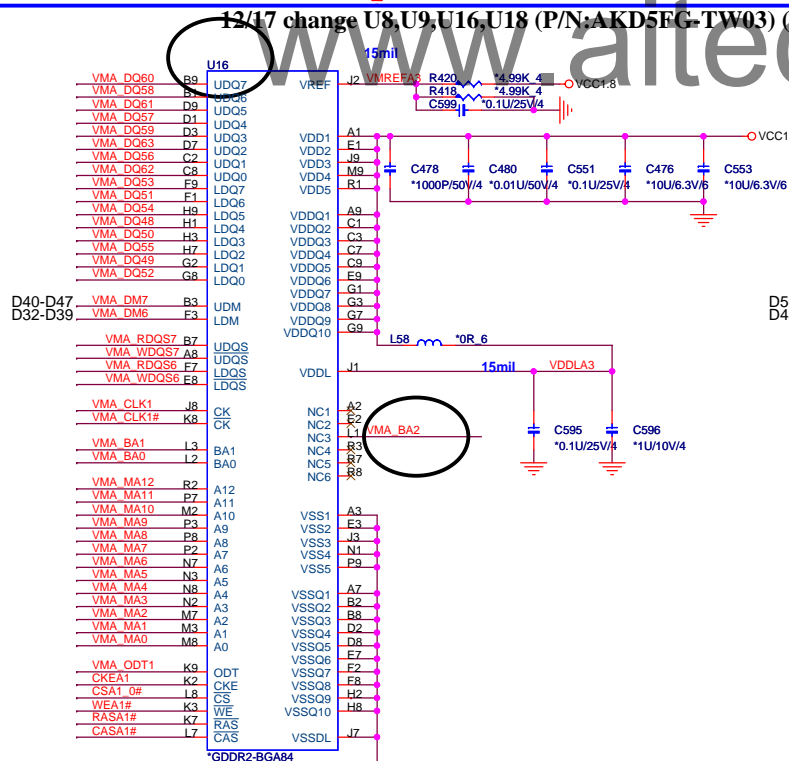
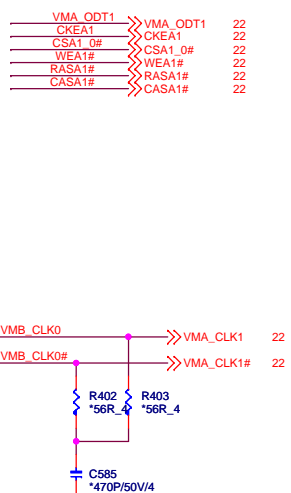


## Channel A-1



25

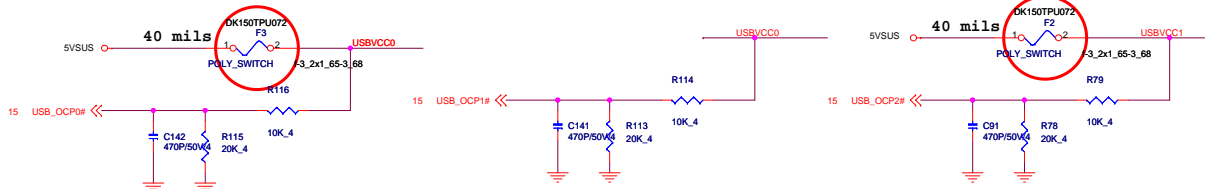
## Channel B-1



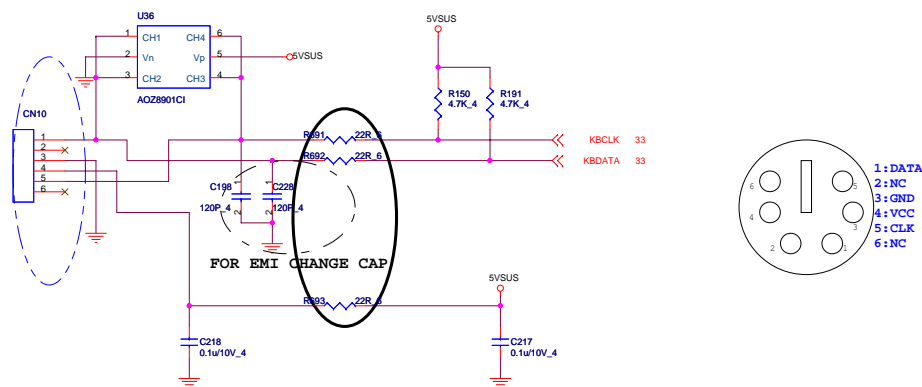
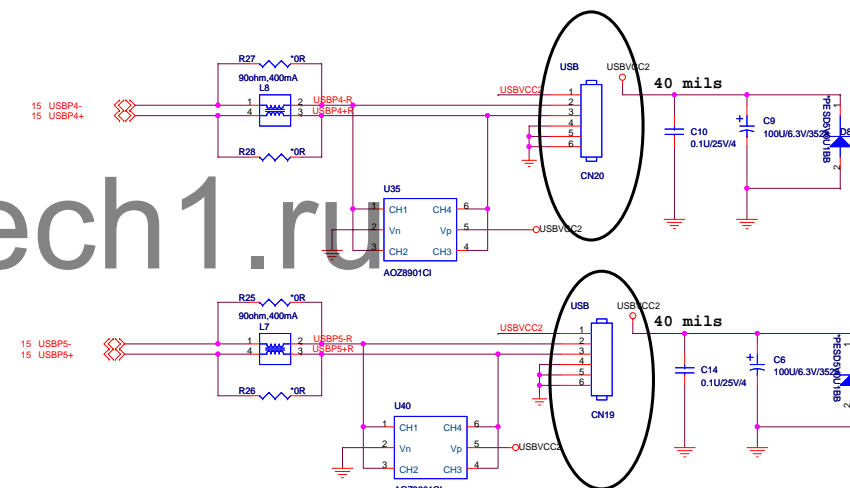
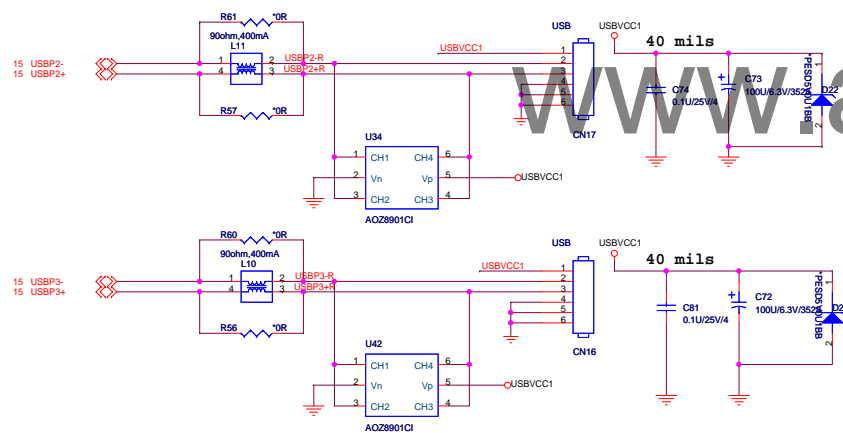
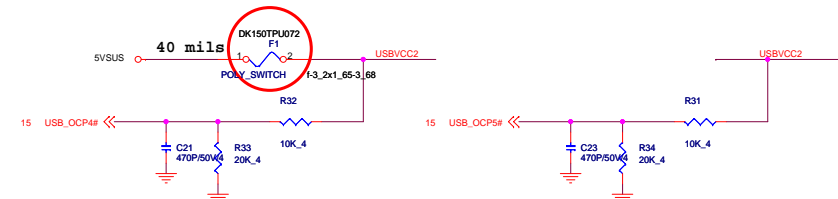
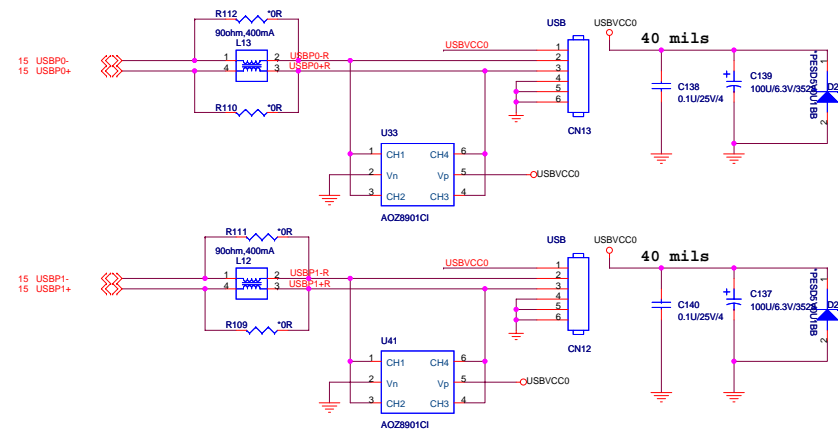




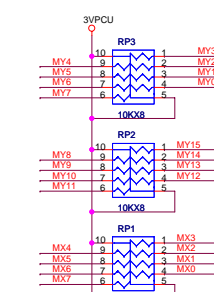
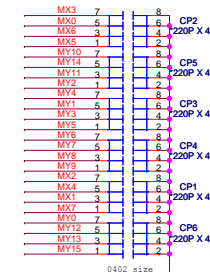
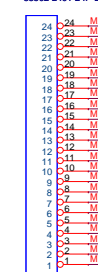


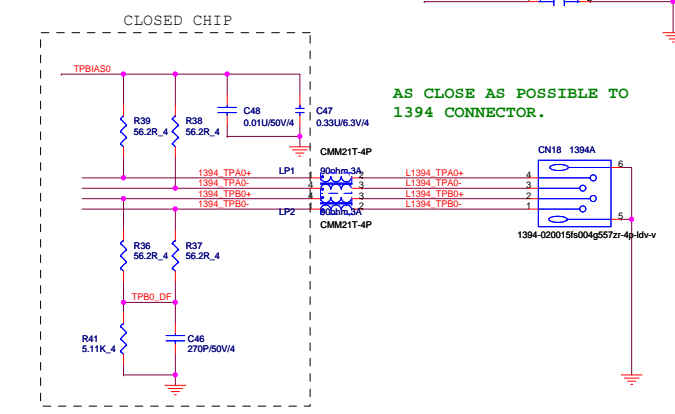


12/01 change F1,F2,F3 P/N (DK150TPU072) and footprint (f-3\_2x1\_65-3\_68)



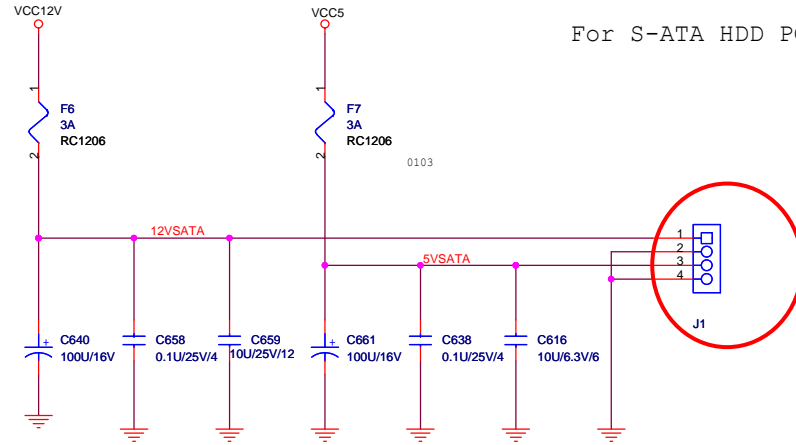
88502-2401-24P-L



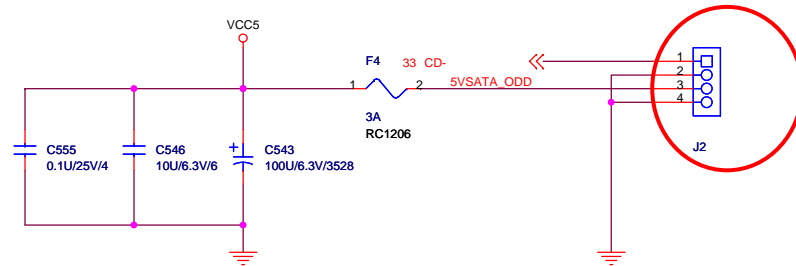


60 mils

For S-ATA HDD POWER

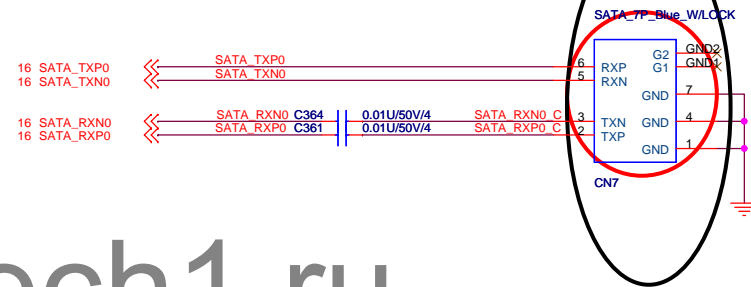


12/02 change J1,J2 PN:DFHS04FR207

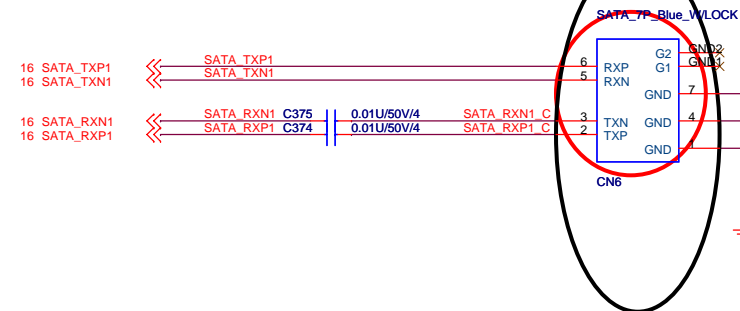


12/05 change CN6,CN7 Footprint sata-aba-sat-010-k07-7p-r

### SATA HDD CONNECTOR



### SATA ODD CONNECTOR



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PROJECT : QU1

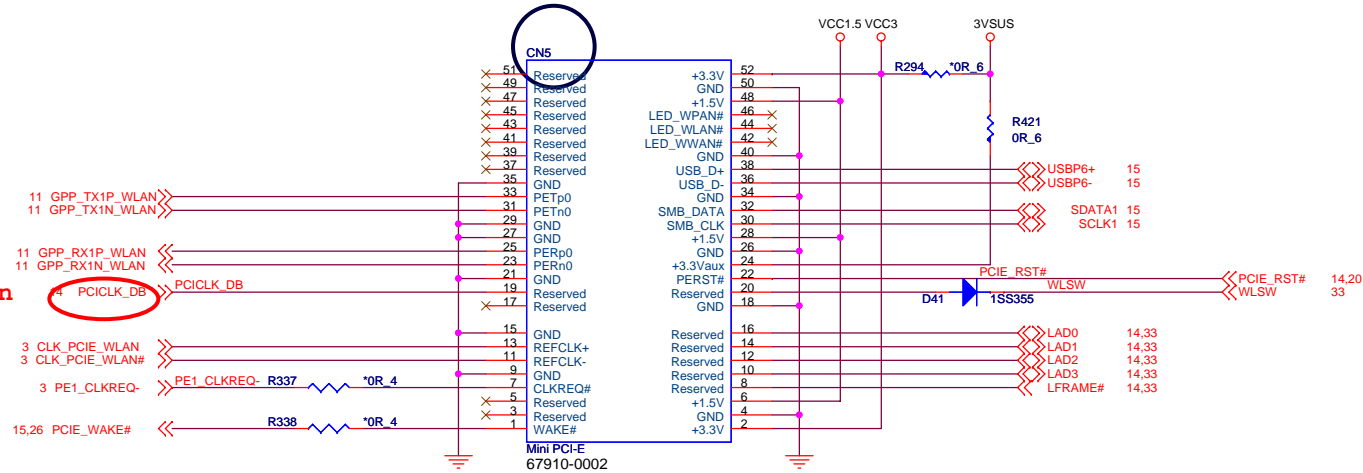


# Mini Card (WLAN)

12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)

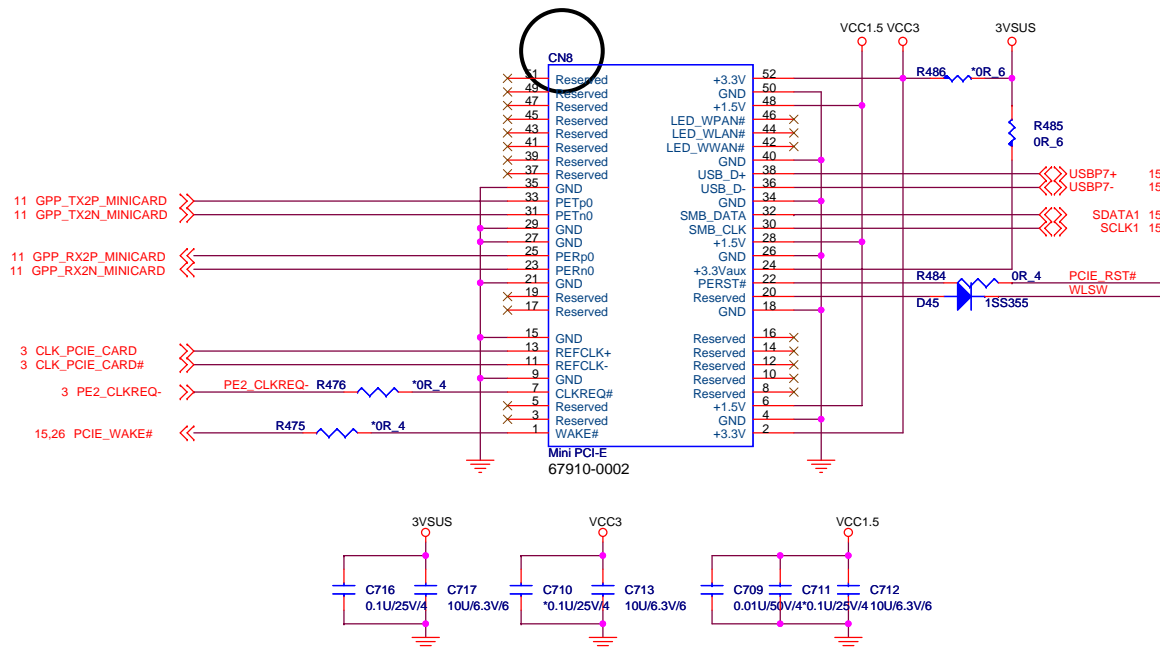
31

12/04 ADD debug port function



# Mini Card (TV Card)

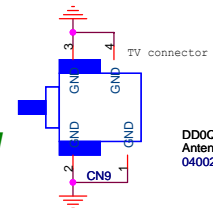
12/26 change CN5,CN8 P/N to meet ACL.(DFHD52MS057)



TV ANTENNA CONNECTOR

ANT. CONNECTOR

Z = 75 OHM



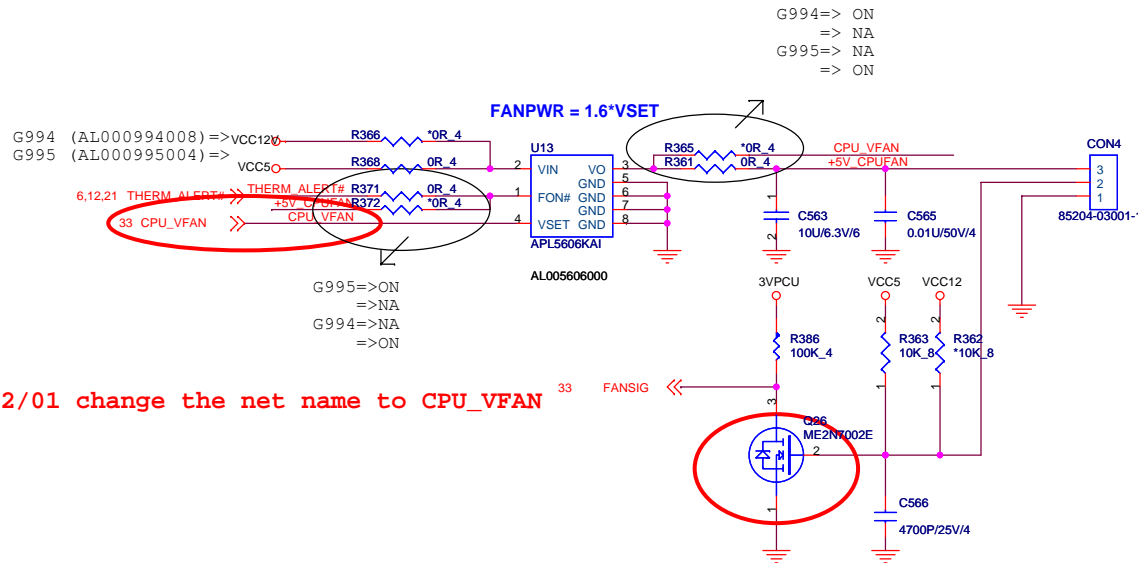
DD0QU1TH000  
Antenna-040023fs001g105-4p-nb3  
040023FS001G105NA



Quanta Computer Inc.

PROJECT : QU1

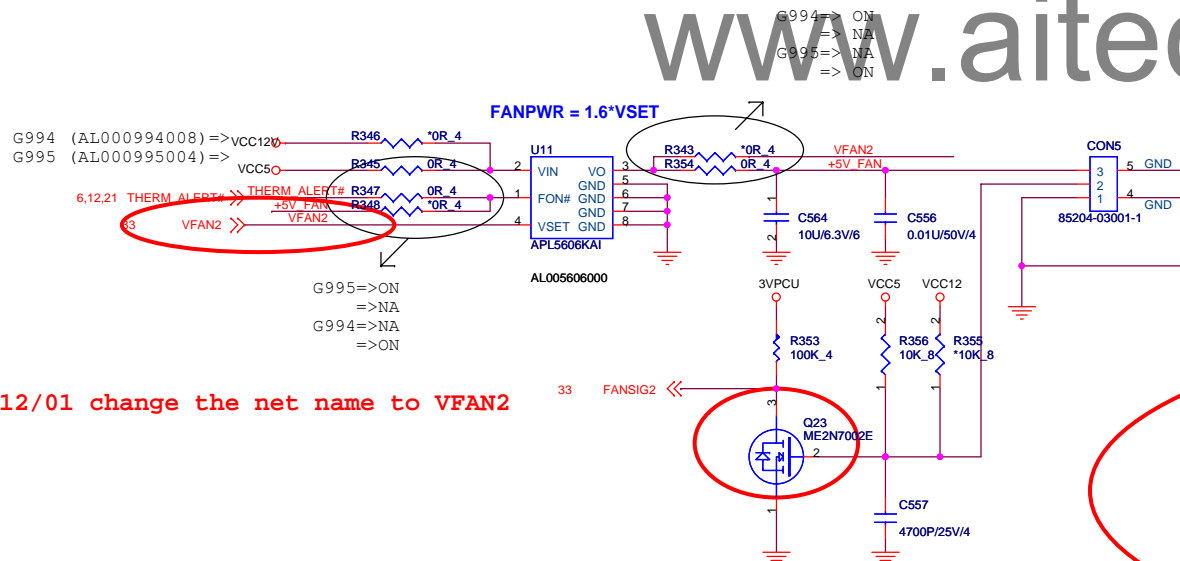
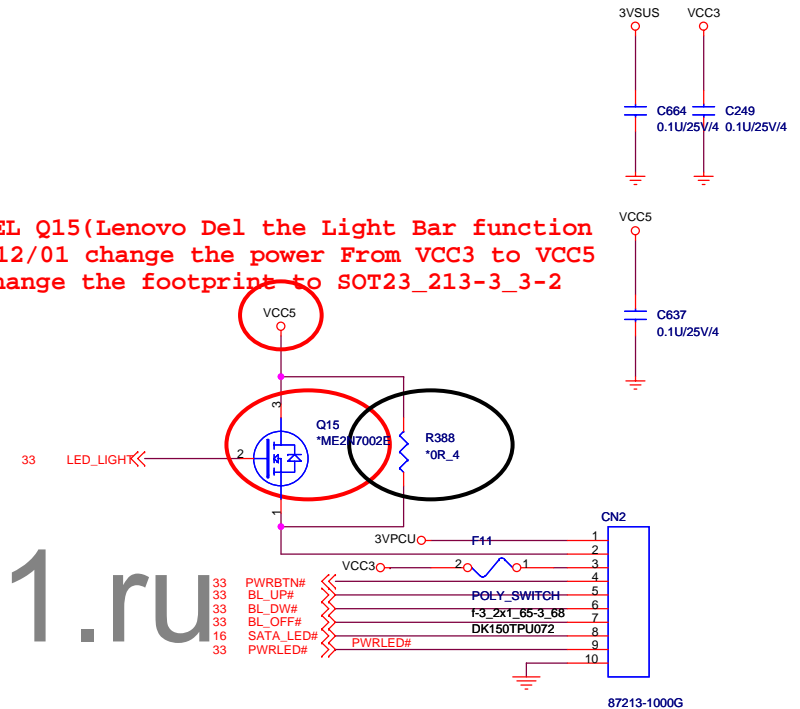
# FAN CONN



12/01 change the net name to CPU\_VFAN

12/01 change the footprint to SOT23\_213-3\_3-2

12/01 DEL Q15(Lenovo Del the Light Bar function  
12/01 change the power From VCC3 to VCC5  
12/01 change the footprint to SOT23\_213-3\_3-2



12/01 change the net name to VFAN2

12/01 change the footprint to SOT23\_213-3\_3-2

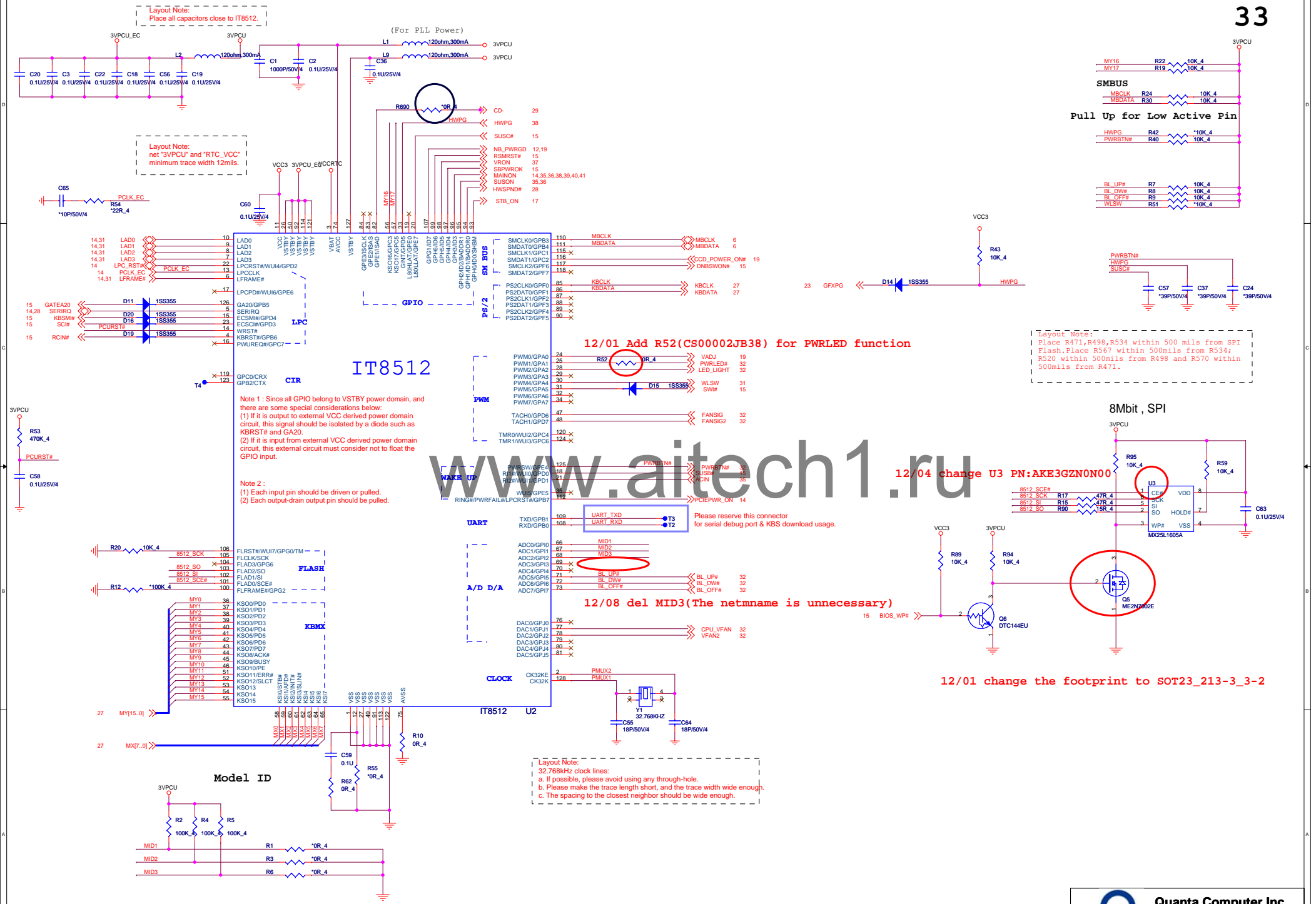
12/01 del U1,Q1,Q3,R13,C11,R21,R11,R29



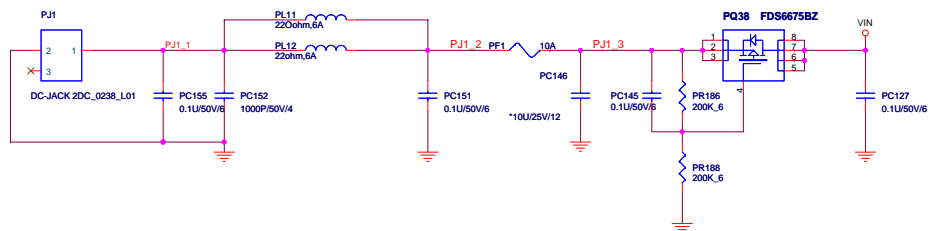
Quanta Computer Inc.

PROJECT : QU1

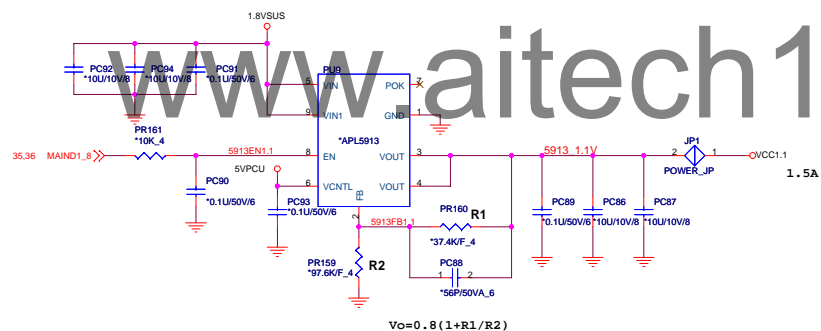


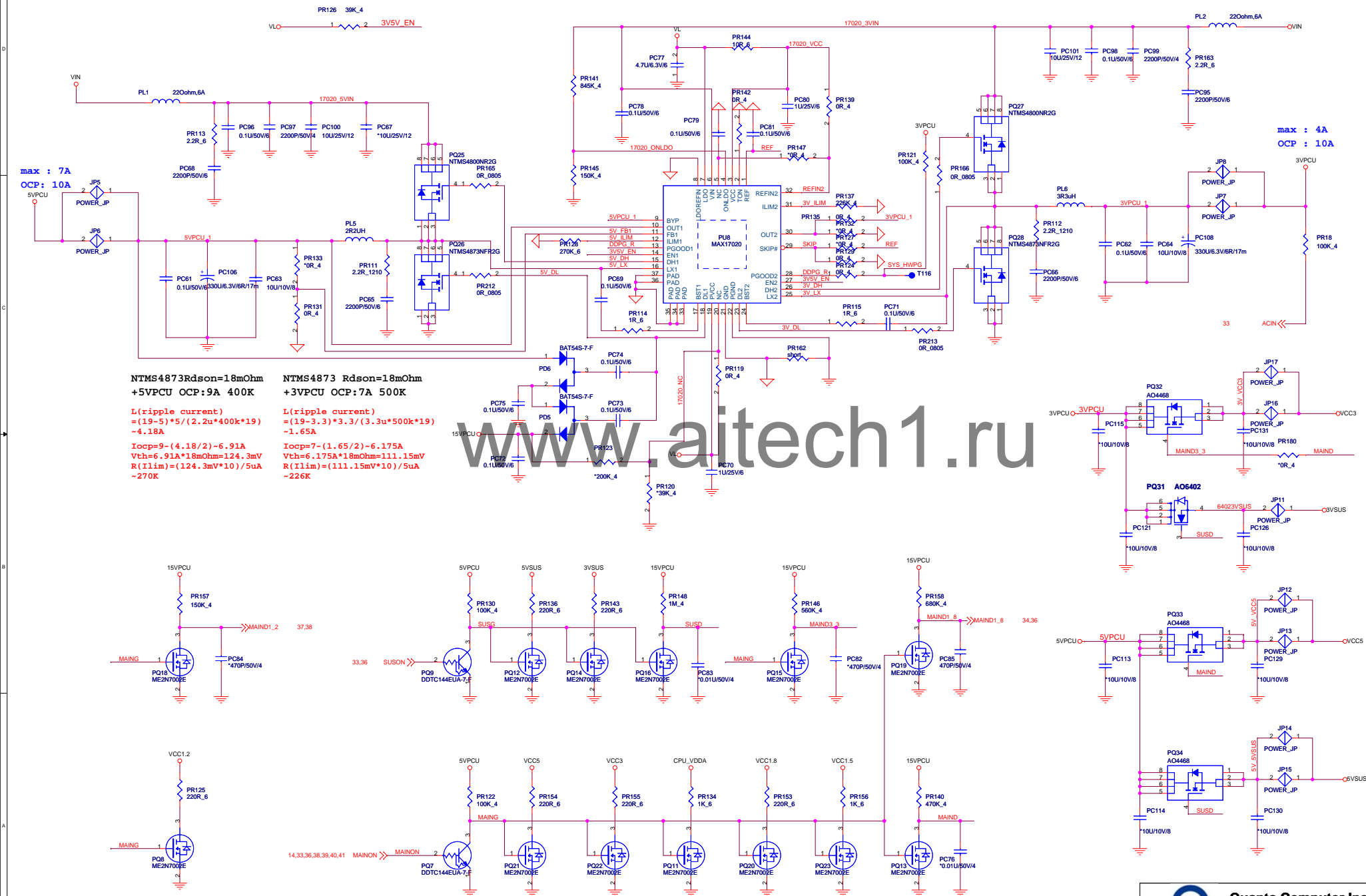


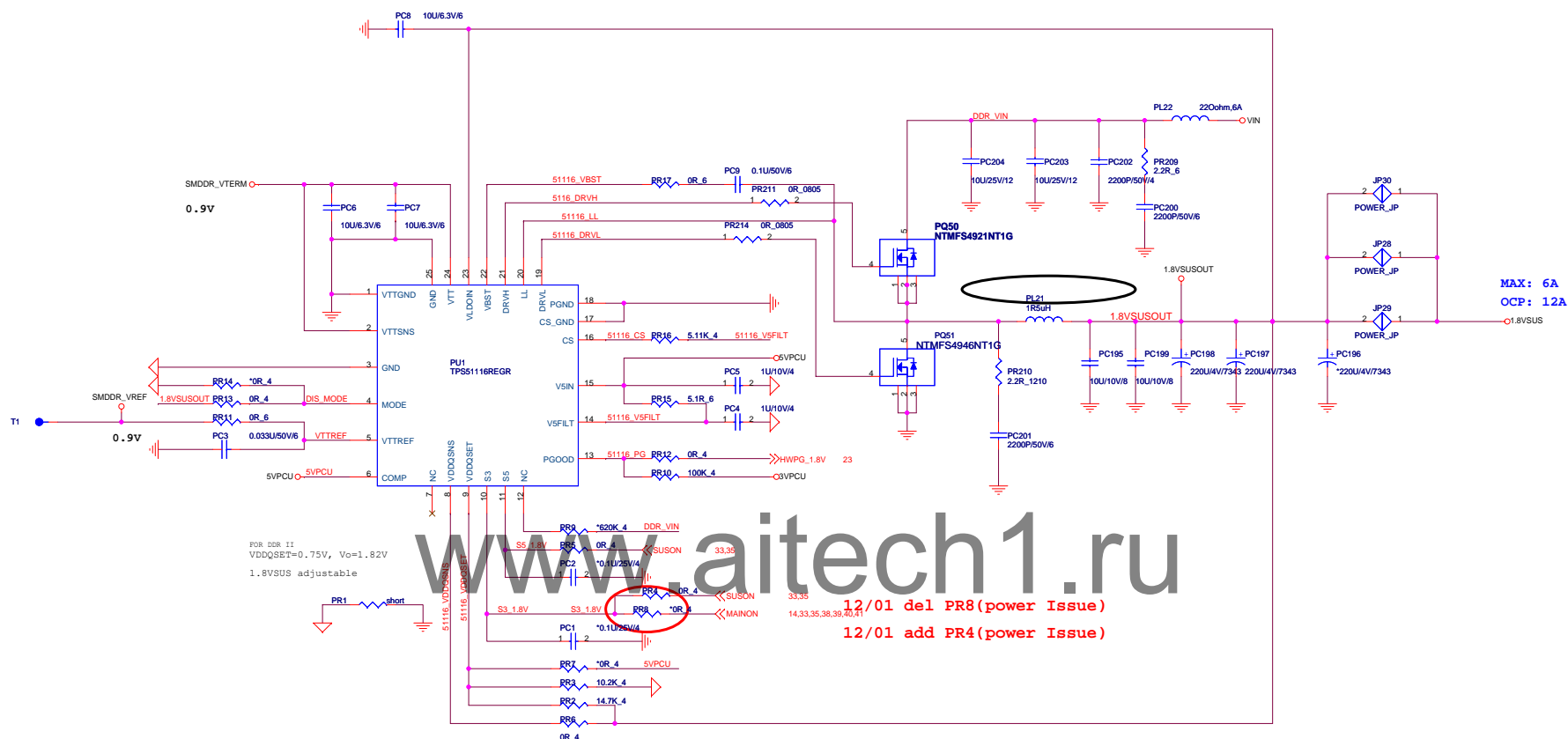
## ACIN



+1.1V







NTMFS4946Rdson=3.8~4.6mOhm

L(ripple current)  

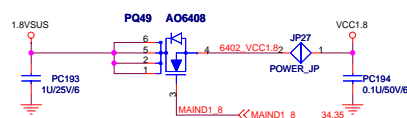
$$= (19 - 1.8) \cdot 1.8 / (1.5 \mu \cdot 400 \text{ k} \cdot 19)$$

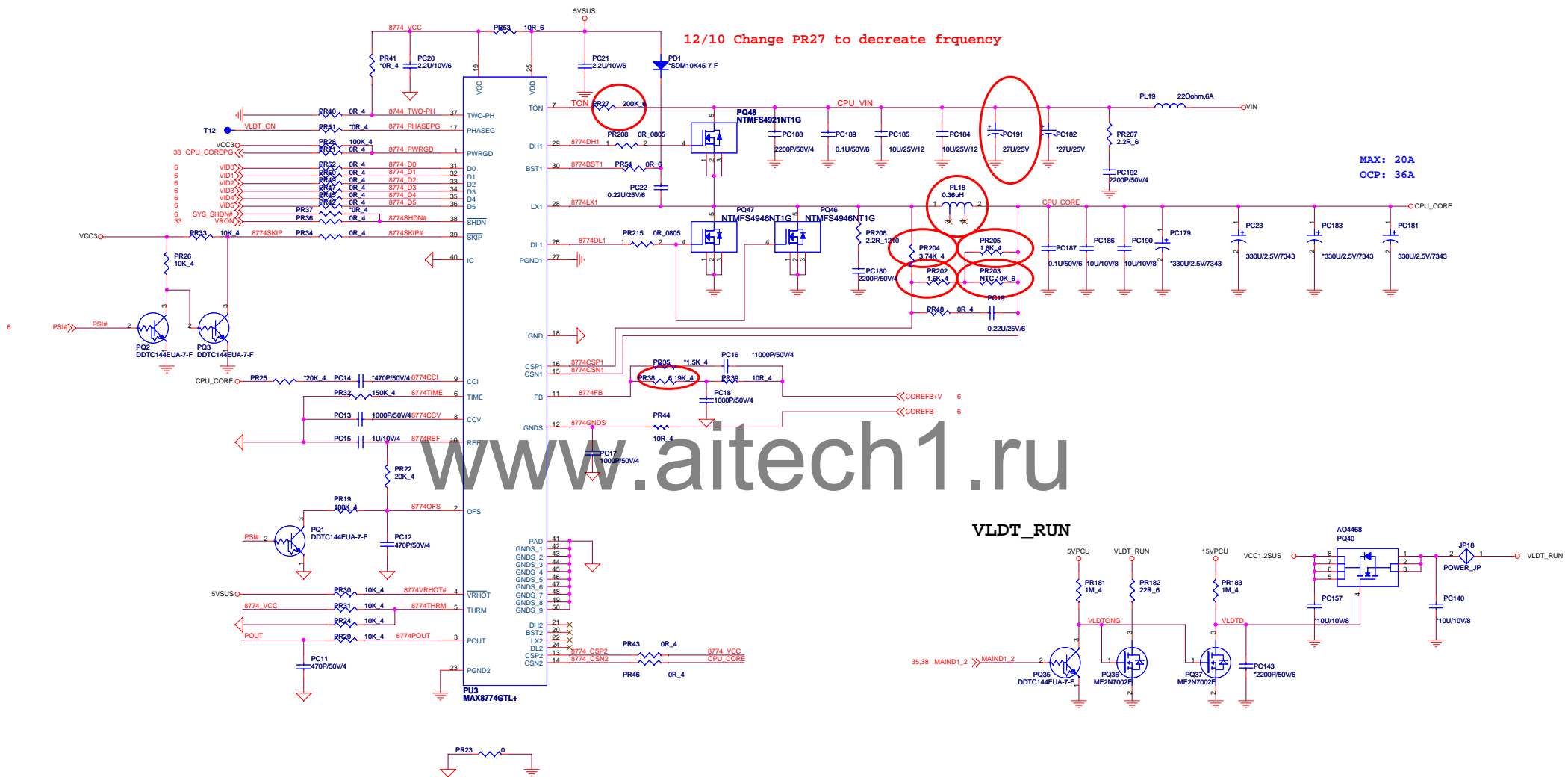
$$\sim 2.72 \text{ A}$$

$$4.6 \text{ m} \cdot (12 - (2.72 / 2)) = \text{RILIM} \cdot 10 \mu \text{ A}$$

$$\text{RILIM} = 5.11 \text{ K}$$

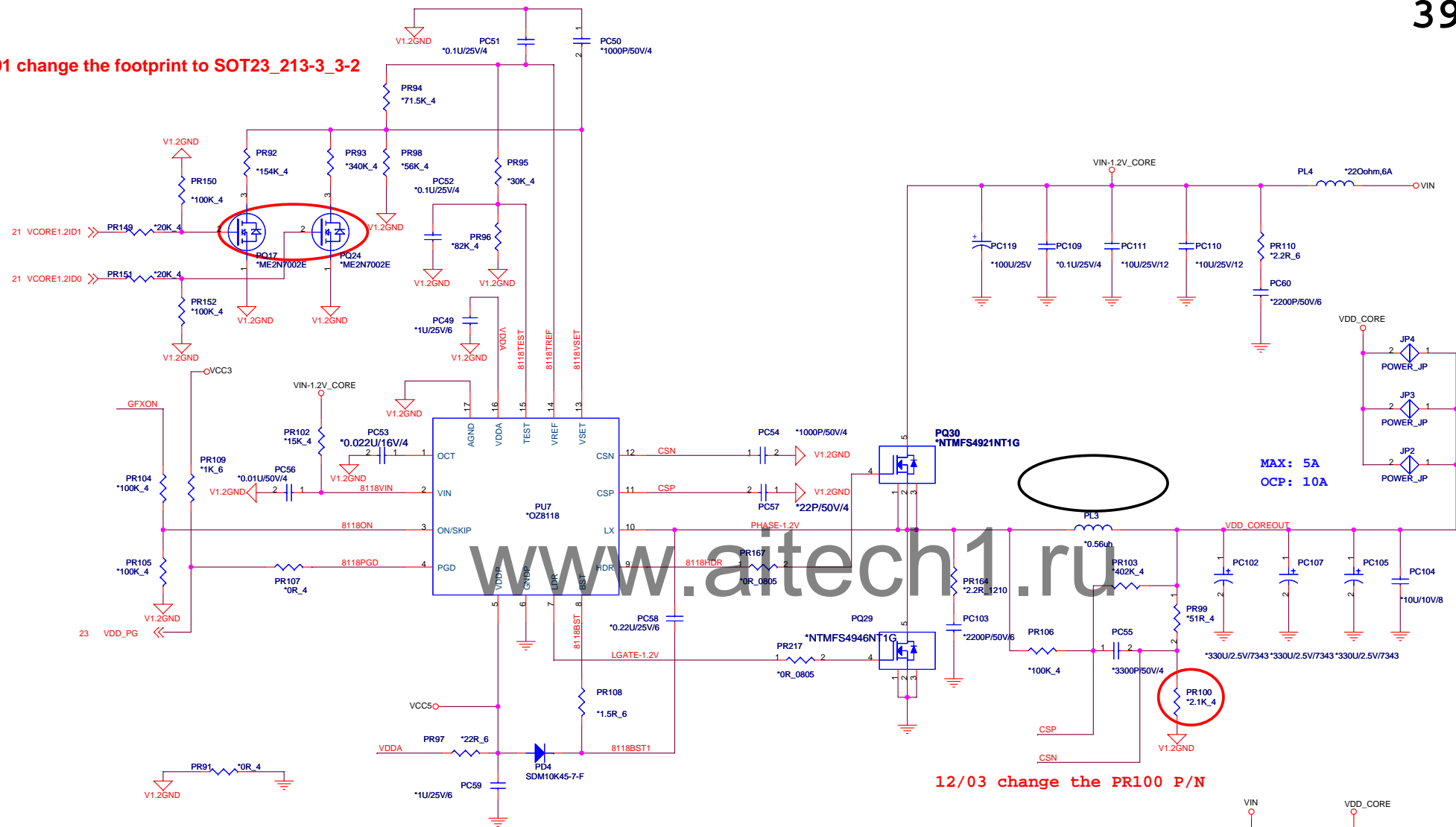
$$((10 \mu \cdot \text{PR67}) / \text{Rdson}) + (\Delta I / 2) = I_{\text{ocp}}$$







**12/01 change the footprint to SOT23\_213-3\_3-2**



M86 TABLE

PR228: 82.5K  
PR229: 226K  
PR230: 374K

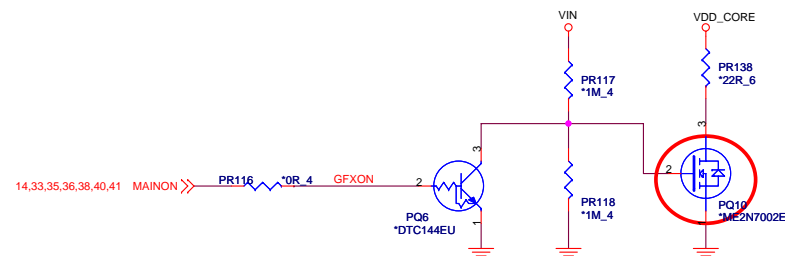
VID[1:0]		
VID1	VID0	
0	0	1.1V
0	1	1.0V
1	0	0.95V
1	1	0.9V

M92 TABLE

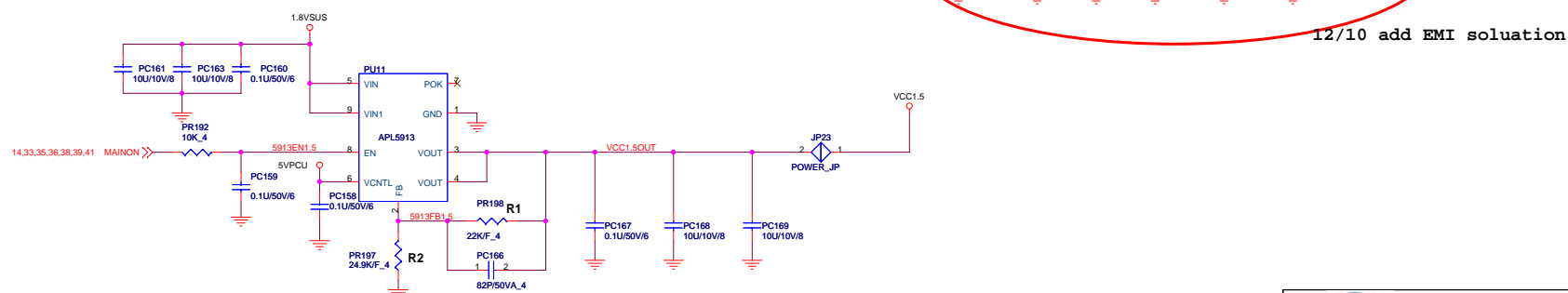
```
PR228: 71.5K
PR229: 154K
PR230: 340K
```

VID[1:0]		
VID1	VID0	
0	0	1.2V
0	1	1.1V
1	0	1.0V
1	1	0.9V

**12/01 change the footprint to SOT23\_213-3\_3-2**

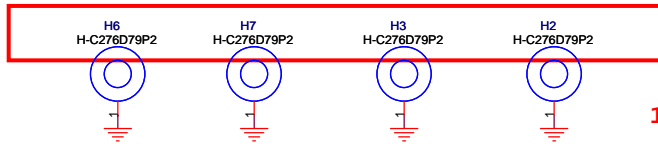
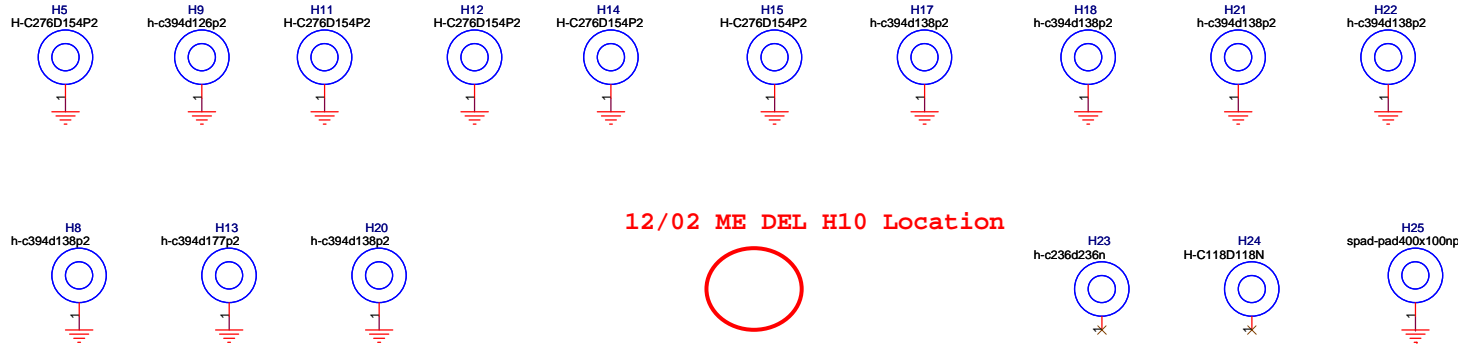






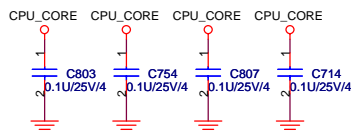
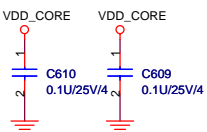
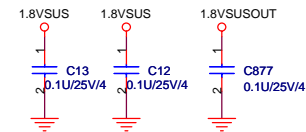
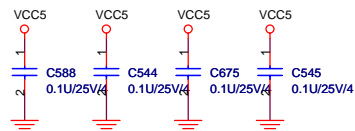
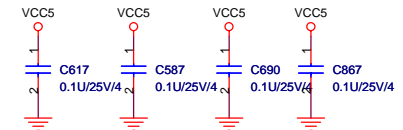
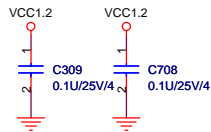
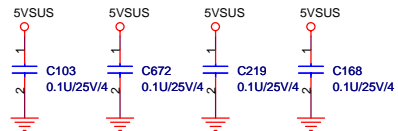
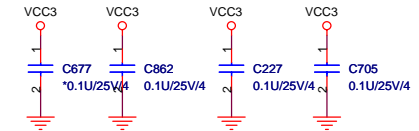
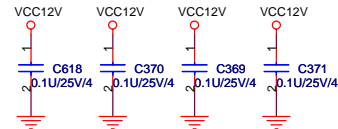
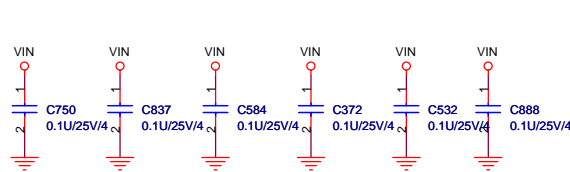
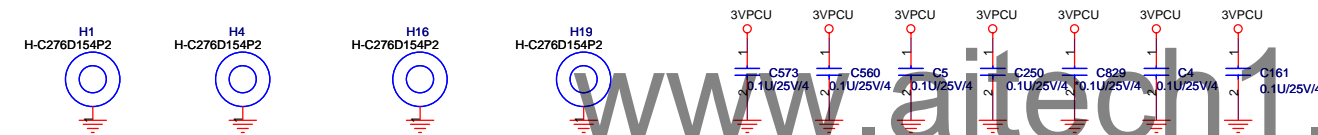






12/02 change H2,H3,H6,H7 footprint to ????(waitting Layout team confirm)

12/02 change H5,H11,H12,H14,H15 footprint to ???(waitting Layout team confirm)



A (EVT) stage :

- Issue**

**Root Cause**
- 1.change Y2 to BG625000885 ==> wrong footprint,change component.
- 2.change F1,F2,F3 to BG625000885 ==> wrong footprint, modify layout.
- 3.change CN5,CN8 to DFHS52FR009 ==> ME request connector move to TOP layer.Top layer have high limit so change component.
4. 12/01 P8----change CN14 footprint (ddr-as0a426-nfst-7f-200p)---SMT issue
5. 12/02 P12----change U7 P/N:AL001032002
6. 12/01 P14---Update the Y5 footprint (XTAL-8\_4X3\_7-5\_5X2\_8)(footprint error)
7. 12/02 P14---Update the BT1 footprint---pindefine error issue
8. 12/05 P15---Change USB Power from Vcc3 to 3VSUS(HW change)
9. 12/02 P16---change Y2 P/N:BG625000885 (footprint not match)
- 10.12/05 P17---del Q9 for RD debug(HW Change)
11. 11/28 P19---del R330,R324(white screen issue)
12. 11/28 P19---exchange D35,D36 to R686,R687(white screen issue)
13. 12/01 P19---change Q2,Q3 footprint to SOT23\_213-3\_3-2(footprint error)
14. 12/01 P20---change Q27,Q31 footprint to SOT23\_213-3\_3-2(footprint error)
15. 12/01 P23---change U12 p/n to AL17SZ08006(Buyer request)
- 16.12/05 P26---Layout update the CN11 footprint
17. 12/01 P27---change F1,F2,F3 P/N (DK150TPU072) and footprint (f-3\_2x1\_65-3\_68)
18. 12/02 P29---change J1,J2 PN:DFHS04FR207(SMT issue)
19. 12/05 P29---change CN6,CN7 Footprint sata-aba-sat-010-k07-7p-r(footprint error)
20. 11/28 P30---add Speaker function(Add R683,R684,C904)
- 21.12/01 P30---change Q2,Q3 footprint to SOT23\_213-3\_3-2(footprint error)
22. 12/01 P30---Exchange MICIN-R and MICIN-L
23. 12/02 P31---change CN5,CN8 P/N because this CONN H=8(DFHS52FS000)
- 24.12/02 P31---12/04 ADD debug port function(Add net--PCICLK\_DB)
25. 12/01 P32---del U1,Q1,Q3,R13,C11,R21,R11,R29
- 26.12/01 P32---change Q15,Q23,Q26 footprint to SOT23\_213-3\_3-2(footprint error)
27. 12/01 P32---12/01 change the net name to VFAN2 and CPU\_VFAN
28. 12/01 P32--- DEL Q15(Lenovo Del the Light Bar function)
29. 12/01 P32---change the power From VCC3 to VCC5
30. 12/01 P33---Add R52(CS00002JB38) for PWRLED function
31. 12/04 P33---change U3 PN:AKE3GZN0N00
32. 12/01 P33---change Q5 footprint to SOT23\_213-3\_3-2
33. 12/01 P36-- ADD PR4,Del PR8(power Issue)
34. 12/01 P37---del PR37(power Issue)
35. 12/03 P37---Change the PR204 ,PR205 P/N
36. 12/01 P38---Del PQ43(Power Issue)
37. 12/01 P38---change PU2 p/n to AL17SZ08006(Buyer request)
38. 12/01 P39---change PQ10,PQ17,PQ24 footprint to SOT23\_213-3\_3-2
39. 12/03 P39---change the PR100 (2.1K); M92/M82 DEL this part.
40. 12/01 P40---del PC150 and Add PC122(near to the VCC12V)
41. 12/01 P41---change PQ4 footprint to SOT23\_213-3\_3-2
42. 12/02 P43--- ME request to Del H10 Location
43. 12/17 change U8,U9,U16,U18 (P/N:DFTJ12FS001) (VRAM change to 400MHZ)

B (DVT) stage :

44. 12/21 P19---del R443,ADD R446(HW LOSE)
45. 12/26 P16---change Y2 P/N to meet ACL.(BG625000737)
46. 12/21 P17---ADD R122 for HW lose
47. 12/23 P19---Add R324 for LCD white screen issue
48. 12/27 P19---Change F8=7A fuse (P/N:DK700WFW006)(LCD INRUSH CURRENT=3A)
49. 12/23 P26---del R587(LAN link issue)
50. 12/29 P26---change CN11 (P/N:DFTJ12FS001)(Change LED color)
51. 12/26 P31---change CN5,CN8 P/N to meet ACL.(DFHD52MS057)
52. 12/29 P12---ADD R689 to link VCC3(Therm\_Alert# must push Hi)

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